EXHIBIT B

DOCKET NO.: 1745950-00120US4
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

STMICROELECTRONICS, INC.
Petitioner

v.

THE TRUSTEES OF PURDUE UNIVERSITY
Patent Owner

IPR2022-00724
U.S. Patent No. 8,035,112

PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 8,035,112
CHALLENGING CLAIMS 2–5, 8, 9, AND 13–16
UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104

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STMicroelectronics, Inc. ("Petitioner") respectfully requests *inter partes* review ("IPR") of claims 2–5, 8, 9, and 13–16 of U.S. Patent No. 8,035,112 (the "'112 patent") (EX1001).

I. INTRODUCTION

The '112 patent is directed to metal oxide semiconductor field effect transistors (MOSFETs) that have self-aligned source contacts. The problem described by the '112 patent and its alleged solution, however, were well-known in the art.

II. MANDATORY NOTICES

A. Real Party-in-Interest

Petitioner STMicroelectronics, Inc. ("ST") is a real party-in-interest. Although STMicroelectronics N.V., ST's parent company, and STMicroelectronics International N.V., which is under common ownership with ST, are not real parties-in-interest under the governing legal standard for making that determination, ST identifies them as real parties-in-interest for purposes of this Petition to avoid any disputes over that issue.

B. Related Matters

According to USPTO records, the '112 patent is owned by The Trustees of Purdue University ("Patent Owner" or "PO"). Petitioner knows of the following co-pending litigations involving the '112 patent: *The Trustees of Purdue University v.*

STMicroelectronics N.V. and STMicroelectronics, Inc., No. 6:21-CV-00727 (W.D. Tex.) and *The Trustees of Purdue University v. Wolfspeed, Inc.*, No. 1:21-CV-840 (M.D.N.C.). Petitioner is challenging claims 1, 6, 7, and 10–12 of the '112 patent in co-pending IPR2022-00309. The earliest date of service on Petitioner in the co-pending litigation was July 20, 2021.

C. Counsel

Under 37 C.F.R. §§ 42.8(b)(3)–(4), Petitioner identifies the following lead and backup counsel, to whom all correspondence should be directed.

Lead Counsel:	Scott Bertulli (Reg. No. 75,886)
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Petitioner consents to service by e-mail on lead and backup counsel.

III. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art ("POSITA") at the time of the earliest claimed priority date of the '112 patent (April 23, 2008) would have had the equivalent of a Bachelor's degree in electrical engineering or a related subject and two or more years of experience in the field of semiconductor devices. Less work experience may be compensated by a higher level of education, such as a Master's Degree, and vice versa. EX1028, ¶23.

IV. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies under 37 C.F.R. § 42.104(a) that the patent for which review is sought is available for *inter partes* review (IPR) and under 37 C.F.R. §§ 42.101(a)–(c) that Petitioner is not barred or estopped from requesting an IPR challenging the patent claims on the grounds identified in this Petition.

V. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED

A. Claims for Which Review is Requested and Grounds on Which the Challenge is Based

Under 37 C.F.R. §§ 42.22(a)(1) and 42.104(b)(1)–(2), Petitioner requests cancellation of claims 2–5, 8, 9, and 13–16 of the '112 patent on the following grounds:

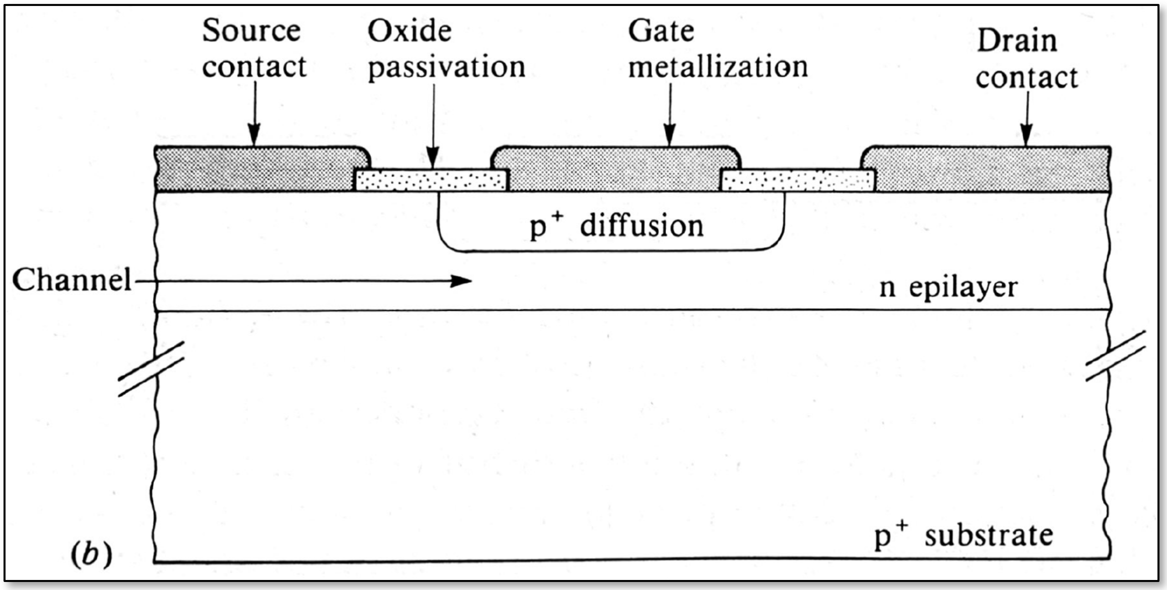
Ground	**References**	**Basis**	**Claims Challenged**
I	*Ueno*	§ 103	2–5, 8, 9, 13, and 14
II	*Ueno* and *Cooper*	§ 103	15 and 16

This Petition, supported by the declaration of Dr. Subramanian (EX1028), demonstrates that there is a reasonable likelihood Petitioner will prevail with respect to cancellation of at least one of the challenged claims. *See* 35 U.S.C. § 314(a).

VI. TECHNOLOGY BACKGROUND

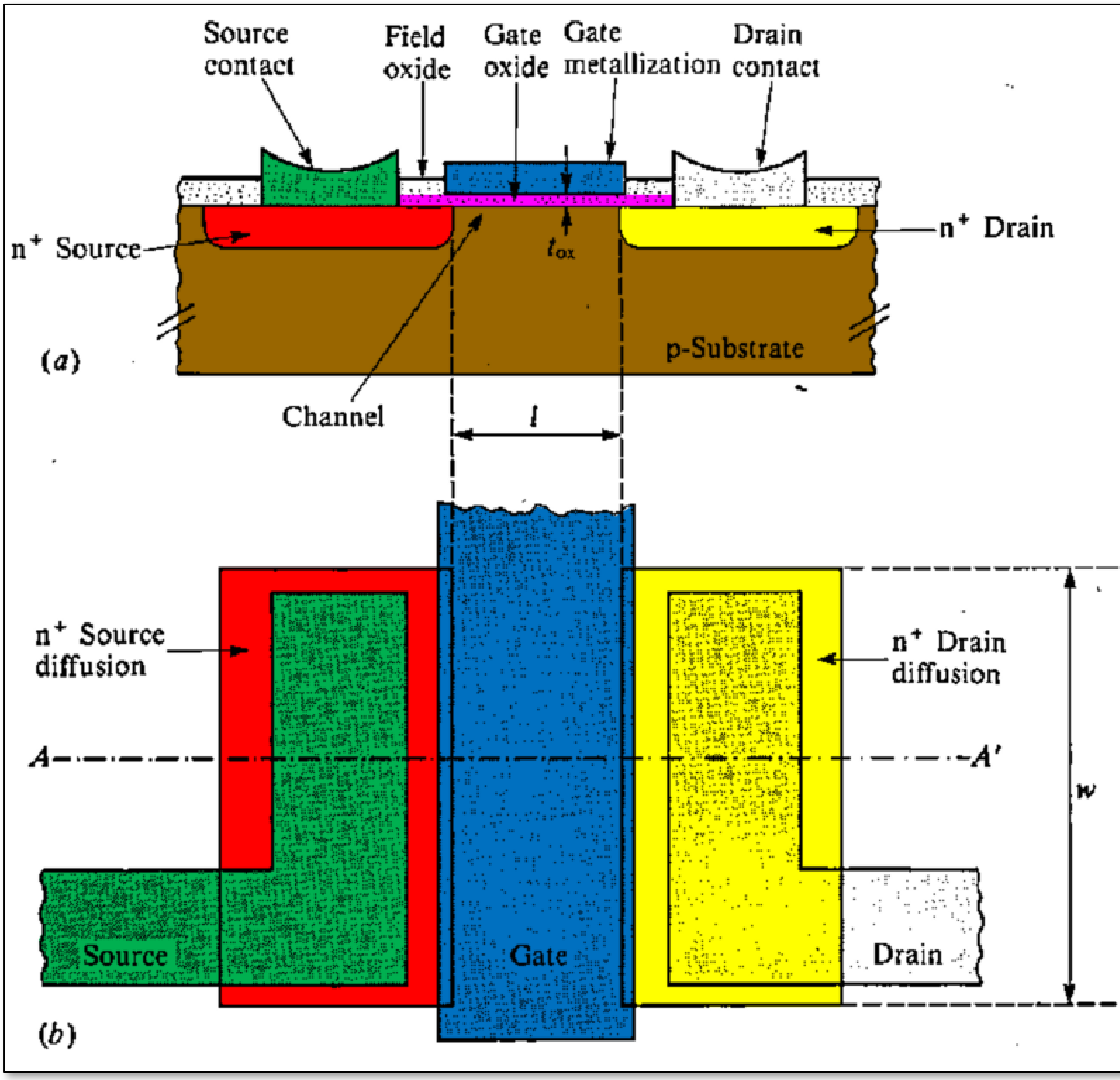
A. Field-Effect Transistor

A field-effect transistor ("FET") is a type of transistor that uses an electric field to control the flow of current in a semiconductor. *See* "Power MOSFETs – Theory and Applications," Duncan A. Grant et al. ("*Grant*"), EX1009, 1. A FET generally includes a source, a drain, and a gate, as *Grant* illustrates in a cross section of a junction field-effect transistor (JFET) in Figure 1.1 (below). *See, e.g.*, *id.*, 2. EX1028, ¶¶24–26.



EX1009, Figure 1.1

"[T]echnological refinements in the early 1960s enabled . . . the metal-oxide-semiconductor field-effect transistor (MOSFET)." EX1009, 5. The difference between a JFET and a MOSFET is "[t]he controlling gate electrode is now separated from the semiconductor by a thin insulating layer of gate oxide, as shown in Figure 1.3." *Id.*; *see also* U.S. Patent No. 5,233,215 ("*Baliga*") (EX1004), 1:45–50. Figure 1.3 (below) shows a MOSFET with the source region annotated in red, the drain region in yellow, the p-type substrate in brown, the gate in blue, the gate oxide in magenta, and the source contact in green. The source contact is often referred to as "source metallization," "source metal," or "source electrode." *See* EX1009, 15–16, Figures 1.12 and 1.13; EX1013, Figure 1, 1:38; EX1004, 2:64. EX1028, ¶27.



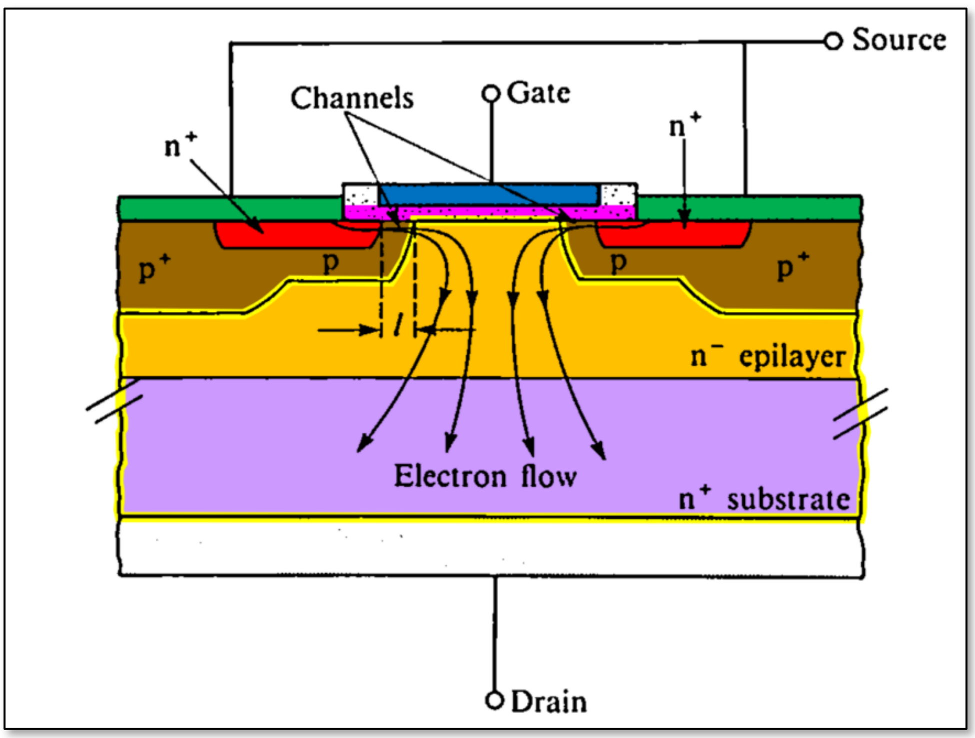
EX1009, Figure 1.3 (annotated)

B. Power MOSFET

The MOSFET became "important in devices designed for power applications." EX1009, 5; *see also* EX1004, 2:14–16. *Grant* notes that "the decision

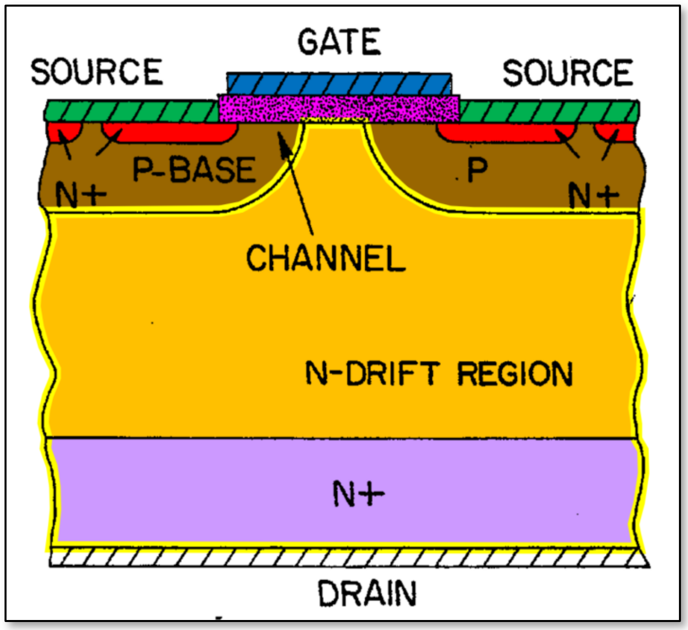
as to what constitutes a power device is quite arbitrary" and the term is applied to "any device capable of switching at least 1 A." EX1009, 5–6. EX1028, ¶28.

Grant found "the planar structure of Figure 1.3 [] unsatisfactory if it is simply scaled up for higher powers." EX1009, 8. One well-known solution was to change from the lateral structure as illustrated in *Grant*'s Figure 1.3 to a vertical structure that uses the substrate material to form the drain region such that "the current flows 'vertically' through the silicon from drain to source." *Id.* This change led to the ***vertical double-diffused MOSFET***, which *Grant* illustrates in Figure 1.11 (below). *Id.*, 13–14. EX1028, ¶29.



EX1009, Figure 1.11 (annotated)

Baliga also illustrates a vertical double-diffused MOSFET in Figure 1 (below). EX1004, 6:12–13. EX1028, ¶30.



EX1004, FIG. 1 (annotated)

The term "double-diffused" derives from a manufacturing technique commonly used to form the n+ source regions and the p-type body region. *See, e.g.*, EX1009, 14; EX1004, 2:35–38. The p-type body region is often referred to as "p-type wells" or "p-base regions." *See, e.g.*, EX1009, 146; EX1004, 2:35, Figure 1. EX1028, ¶31.

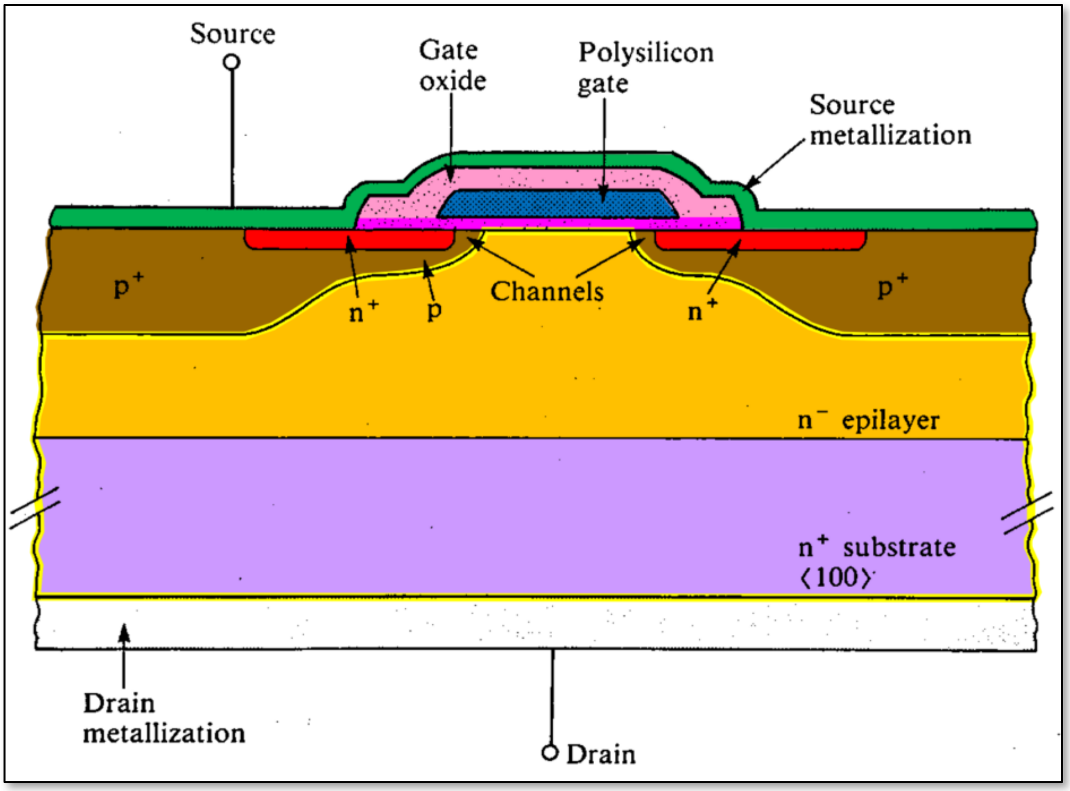
In *Grant*'s Figure 1.11 and *Baliga*'s Figure 1 above, the source regions are annotated in red, the p-type body regions in brown, the gate in blue, the gate oxide in magenta, and the source contacts in green. The drain region (yellow) comprises the substrate (lavender) and the epilayer (orange). Electrons flow from the source

to the drain through the channels formed in the p-type wells, the epilayer, and the substrate. The epilayer is often referred to as the "drift region." *See, e.g.*, EX1009, 74. EX1028, ¶32.

According to *Grant*, "[a] development that was of great importance in integrated-circuit MOS technology in the 1970s was the ***use of heavily doped polycrystalline silicon***, rather than aluminum, ***to form the gate electrode***." EX1009, 14–15.[1] Power FETs achieved several advantages as a result, including: simplified connection metallization because "***an oxide layer can be formed over the poly-Si, and the source metallization may then be extended over the whole of the upper surface***;" better control of the threshold voltage; and self-alignment of the source with the gate edge. *Id.* EX1028, ¶33.

Grant's Figure 1.12 (below) shows the source region in red, the p-type body regions in brown, the gate in blue, the gate oxide in magenta, the oxide layer formed over the polysilicon gate in pink, and the source metallization in green. The drain region (yellow) comprises the substrate (lavender) and the epilayer (orange). As is apparent, the source metallization extends over the entire upper surface. EX1028, ¶34.

[1] Unless otherwise noted, all emphasis has been added.

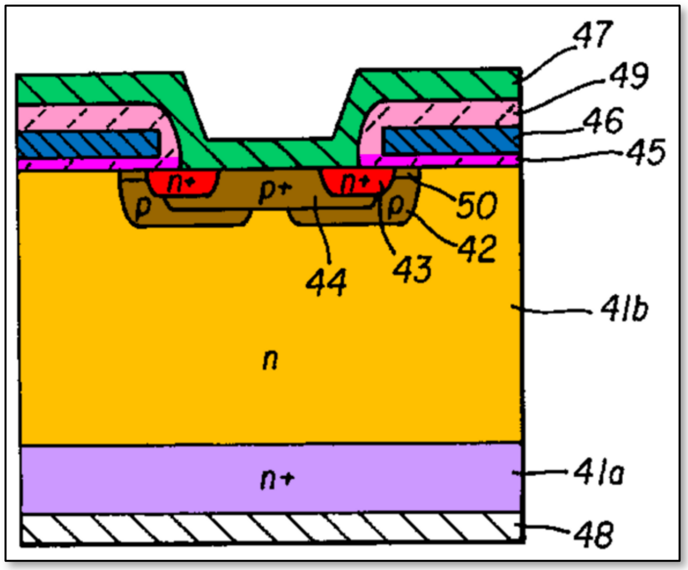


EX1009, Figure 1.12 (annotated)

C. Plurality of Cells

Prior art references conventionally illustrate a cross-sectional view of one unit cell of a power MOSFET (*e.g.*, as in *Grant*'s Figures 1.11 and 1.12 and *Baliga*'s Figure 1, all reproduced above). U.S. Patent No. 6,238,980 to Ueno ("*Ueno*") (EX1003) shows a similar example of a cross-sectional view of one unit cell of a power MOSFET in Figure 1 (below). *See* EX1003, 7:65–66. A POSITA would have appreciated that, while the unit cells of the MOSFETs in *Grant*'s Figures 1.11 and 1.12 and *Baliga*'s Figure 1 are drawn centered on their gates (blue), *Ueno*

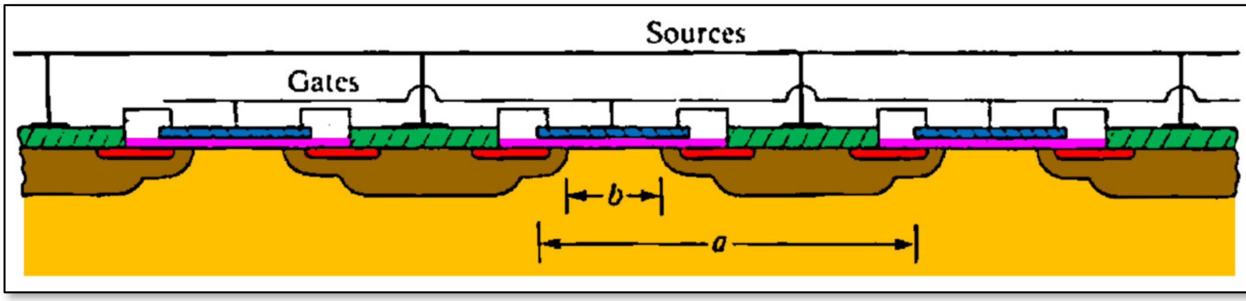
illustrates the unit cell of its MOSFET shifted one half unit so it is centered on its base region (brown). In this view, two gates are visible. EX1028, ¶35.



EX1003, FIG. 1 (annotated)

Regardless of how a unit cell is illustrated, a POSITA would have understood that a power MOSFET device may include a plurality of adjacent unit cells, laid out next to each other at a regular pitch. *See, e.g.*, EX1009, Figure 1.13; EX1013, Figure 1; *see also* EX1009, 383 ("A vertical diffused power MOSFET consists of many parallel cells . . ."); *id.* at 15; EX1003, 8:32–33 ("The pitch of unit cells as shown in FIG. 1 is about 25 μm."). *Grant* explains the well-known concept of pitch, stating that "VDMOS FET gates may be laid out as linear arrays, interdigitated with the source, as shown in Figure 3.9*a* . . . where *a* is the pitch of the array." EX1009, 455. An excerpt of *Grant*'s Figure 3.9*a* below illustrates the pitch *a*. *Grant* illustrates other well-known arrays of unit cells laid out at a regular pitch that have similar

cross sections as shown in Figure 3.9a. *See id.* at 70–73, Figure 3.9; *see also id.* at 16, Figure 1.13. EX1028, ¶36.



EX1009, Figure 3.9*a* (excerpted and annotated)

D. Silicon Carbide (SiC)

Historically, power MOSFETs were fabricated using monocrystalline silicon (*i.e.*, a single-crystal silicon). By the early 1990s, silicon carbide (SiC) was known to be particularly well suited for such devices. EX1004, 4:22–27. SiC was known to allow SiC power devices to operate at higher temperatures, higher power levels and with lower specific on resistance than conventional silicon-based power devices." *Id.*, 4:31–34; *see also* U.S. Patent No. 5,510,281 ("*Ghezzo*") (EX1010), 1:52–56. EX1028, ¶37.

Baliga teaches that "power MOSFET such as the above described DMOSFET . . . can be readily translated into silicon carbide using known manufacturing techniques," *e.g.*, by using higher temperature, and longer, diffusions to compensate for the lower diffusion coefficient in silicon carbide. EX1004, 4:35–43. *Ghezzo*, which issued in 1996 over a decade before the '112 patent was filed, also teaches

that "[a] method of implementing vertical power SiC transistor is to replace the conventional double-diffusion with an edge-shifted double ion implantation sequence to overcome the problem of very small dopant diffusivity in SiC" and that "[t]he channel is formed by successive ion implantation of an acceptor atom (such as boron or aluminum) and a donor atom (such as nitrogen or phosphorous) to form the base and source regions, respectively." EX1010, 1:56–63. Accordingly, SiC power MOSFETs are often referred to as "double-implanted" MOSFETs. *Ghezzo* explains that "[t]he implantations precede the gate electrode formation" because "[t]he self-alignment procedure used for conventional silicon devices cannot be used for SiC because known metal-oxide-semiconductor structures fail to withstand the high temperature of implant activation of about 1500° C." *Id.*, 2:2–12. That is, implants are activated to form source and drain regions when the surface of the wafer is bare. *See, e.g.*, EX1003, 10:20–25, Figures 3(a), 3(b). EX1028, ¶38.

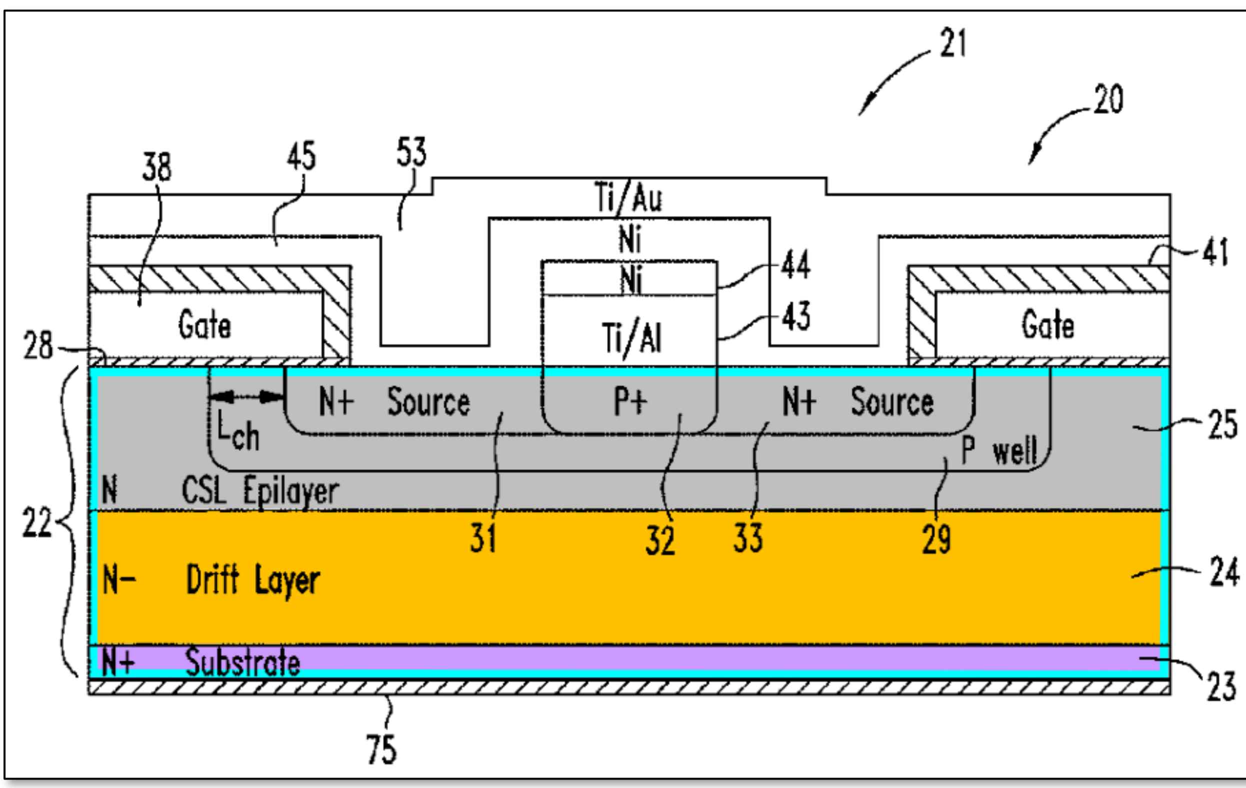
Vertical power MOSFETs made with SiC were well-known long before the '112 patent. *Id.*, ¶39.

VII. THE '112 PATENT

A. Alleged Invention

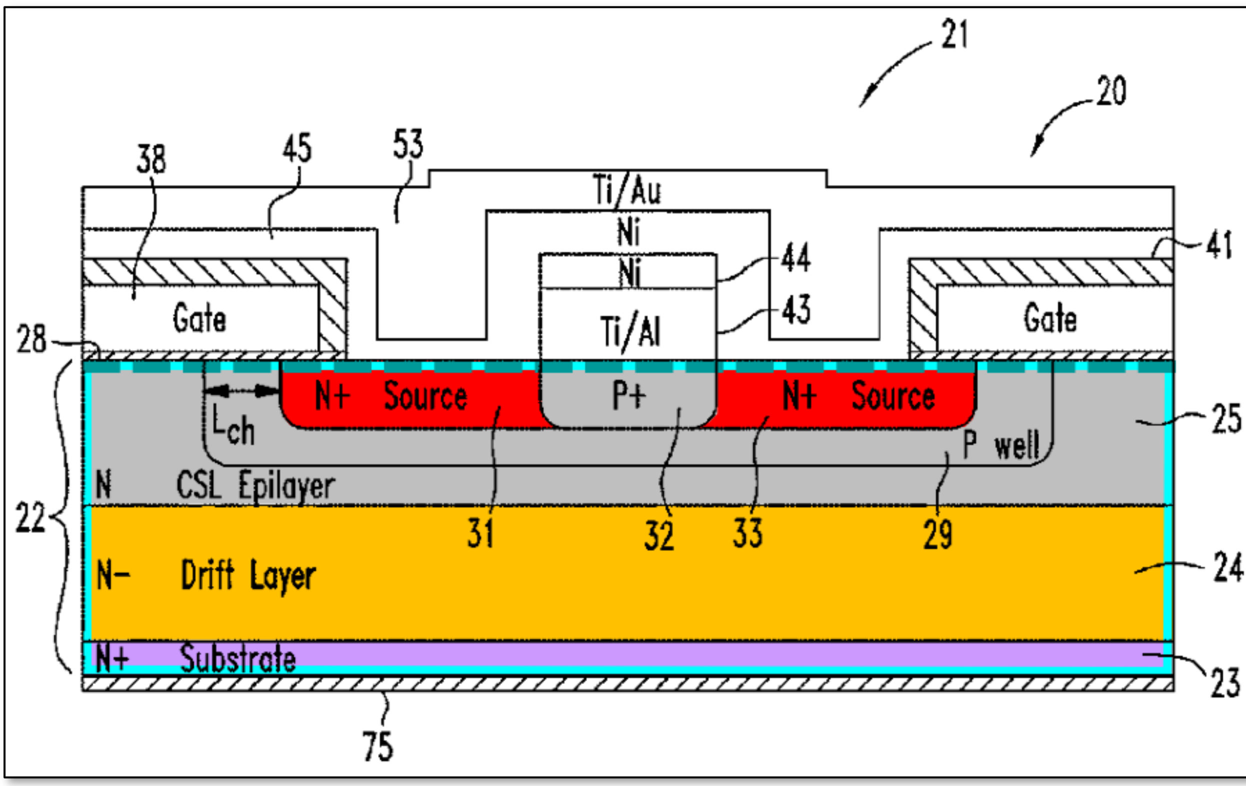
The '112 patent is generally directed to "high voltage power MOSFETs." EX1001, 2:24–26. The '112 patent describes a vertical MOSFET, having a well-known structure as depicted in Figure 3 (below). *Id.*, 1:44; 2:49–50, 3:60–63, Figure

3. The MOSFET 21 of Figure 3 includes a SiC **wafer having a substrate body 22** (cyan below). *Id.*, 4:8–15, 9:26. The **substrate body 22** includes a **substrate 23** (lavender), a **drift layer 24** (orange) formed atop **substrate 23**, and a **current spreading layer (CSL) 25** (grey) formed atop **drift layer 24**. *Id.*, 4:8–11, 4:24–26. **Substrate 23** is heavily doped with N-type impurities to an "N+" concentration, **drift layer 24** is lightly doped to an "N−" concentration, and **CSL 25** "is more heavily doped than **drift layer 24**, but not as heavily doped as **substrate 23**." *Id.*, 4:22–28. The '112 patent illustrates the **CSL 25** as having an "N" concentration. *Id.*, Figures 3–8. EX1028, ¶40.



EX1001, FIG. 3 (annotated)

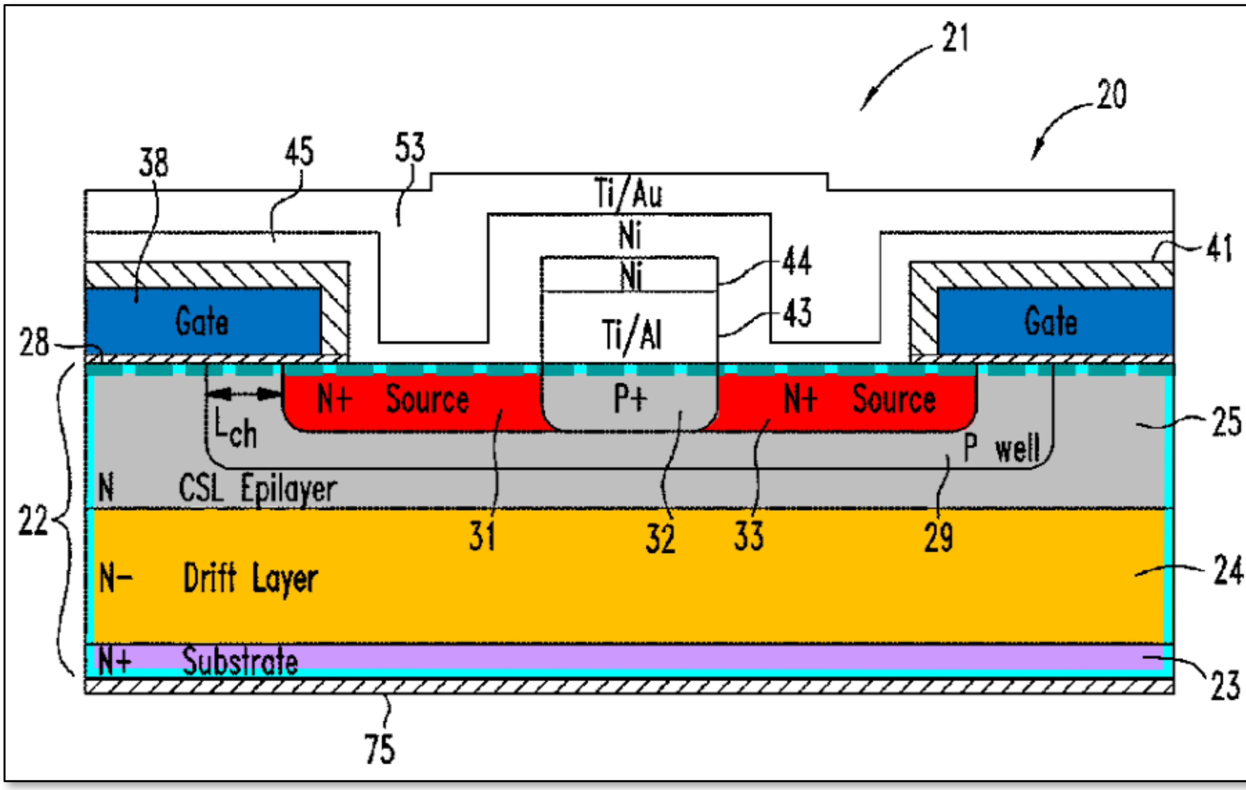
The ’112 patent’s MOSFET 21 can include a number of implants such as the pair of “heavily doped N+ implant **source regions 31 and 32**”[2] (red below). *Id.*, 4:8–11, 4:51–53. The **source regions 31 and 32** are formed adjacent the **top surface 28** (identified with a dashed teal line) of the **substrate body 22**. *E.g.*, *id.*, 4:9–11; 8:41–42; 8:57–58; 9:6–7; 9:27–28. In the embodiment of Figure 3, the **source regions 31 and 32** are defined in the CSL 25. *Id.*, 10:39–41. EX1028, ¶41.



EX1001, FIG. 3 (annotated)

[2] Reference numerals 32 and 33 are interchanged in Figure 3.

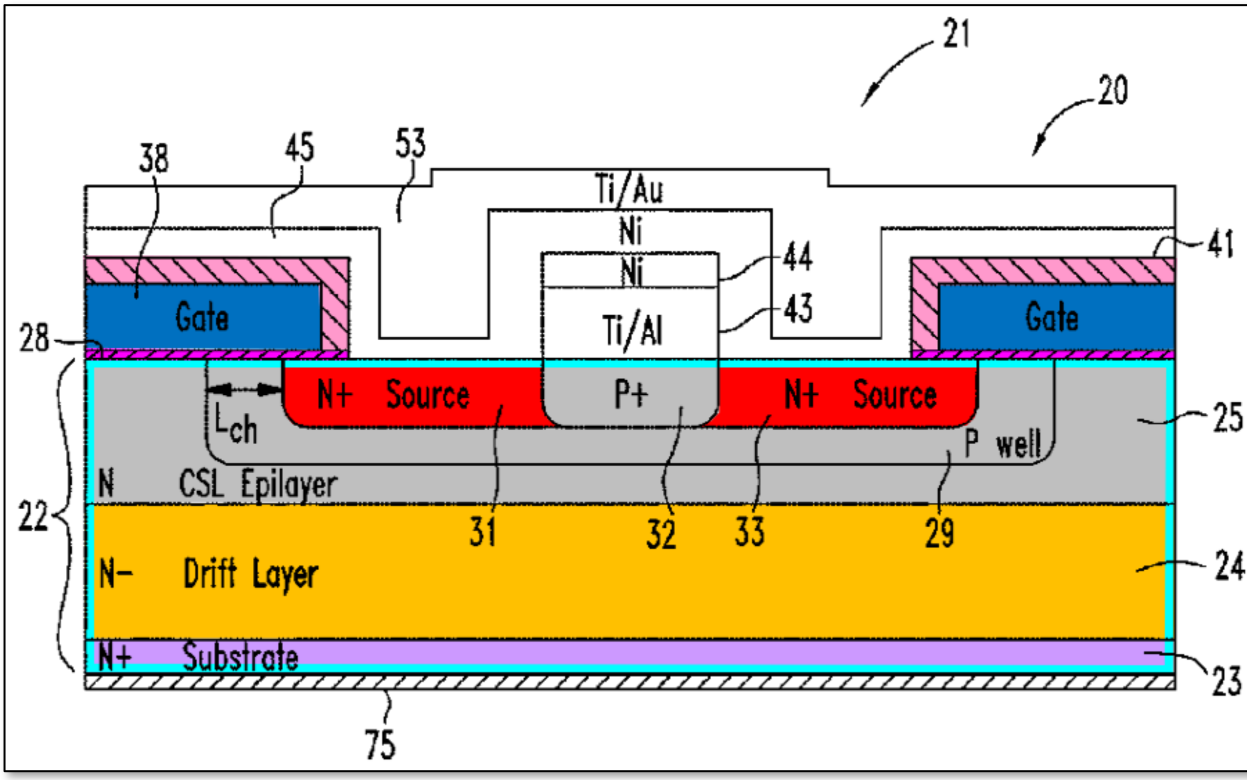
Formed atop the **upper surface 28** are polycrystalline silicon (*i.e.*, polysilicon) **gates 38** (blue below). *Id.*, 4:66–5:2. EX1028, ¶42.



EX1001, FIG. 3 (annotated)

Each **gate 38** is "surrounded along its top, bottom, left and right sides by an insulating layer of silicon dioxide 41," referred to as the "oxide layer 41." *Id.*, 5:2–10. Figure 3 illustrates and the '112 patent's claims describe that the **oxide layer over the top and sides** (pink) of each **gate 38** is ***thicker*** than the **oxide layer beneath** (magenta) the **gate 38**. *E.g., id.*, 8:33–36, 9:37–39, Figure 3. "Because it is much thicker, the oxide over the polysilicon gate is not completely removed"

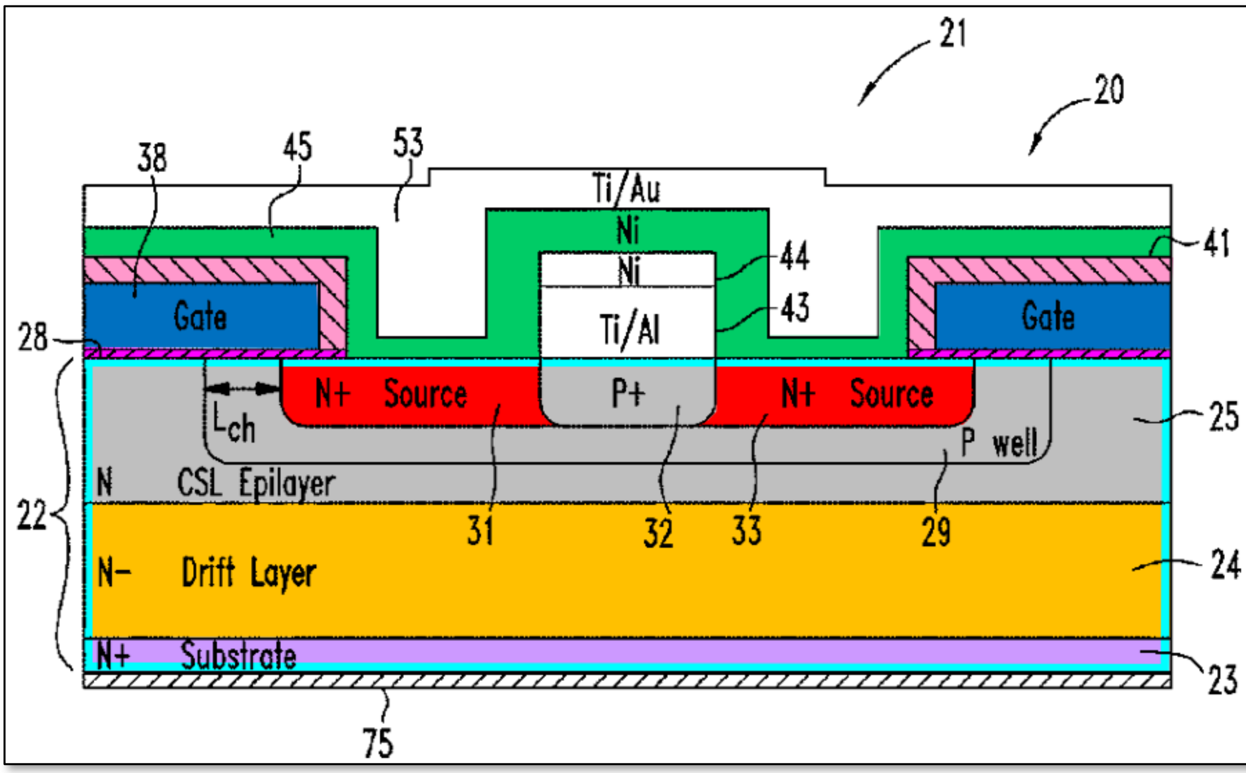
during a later etching step in the fabrication process, thus leaving behind "an insulating layer over and around the polysilicon gate." *Id.*, 6:1–4. EX1028, ¶43.



EX1001, FIG. 3 (annotated)

An ohmic **contact metal 45** (green) is then "formed over the entire MOSFET 21, overlapping the polysilicon **gate 38**, but insulated from it by the thick **oxide 41 on the top and sides** thereof." *Id.*, 5:5–8. "Because **gate 38** is completely surrounded by insulating **oxide layer 41**, its positionment relative to **source contacts 31 and 32** is much less critical, and it cannot detrimentally come in contact with any portion of the Ni **metal contact 45** due to any mask misalignment during processing." *Id.*, 5:9–13. Further, "the deposition of Ni **metal contact 45** over the

entire MOSFET 21 … makes conformal, direct and self-aligning contact … most importantly, with N-**source implants 31 and 32**." *Id.*, 5:19–25. Although the '112 patent describes forming a Ti/Al contact metal 43, and a Ni contact metal 44 atop the P+ base 33 (*see* center of Figure 3 below), none of these features are claimed by the '112 patent. EX1028, ¶44.

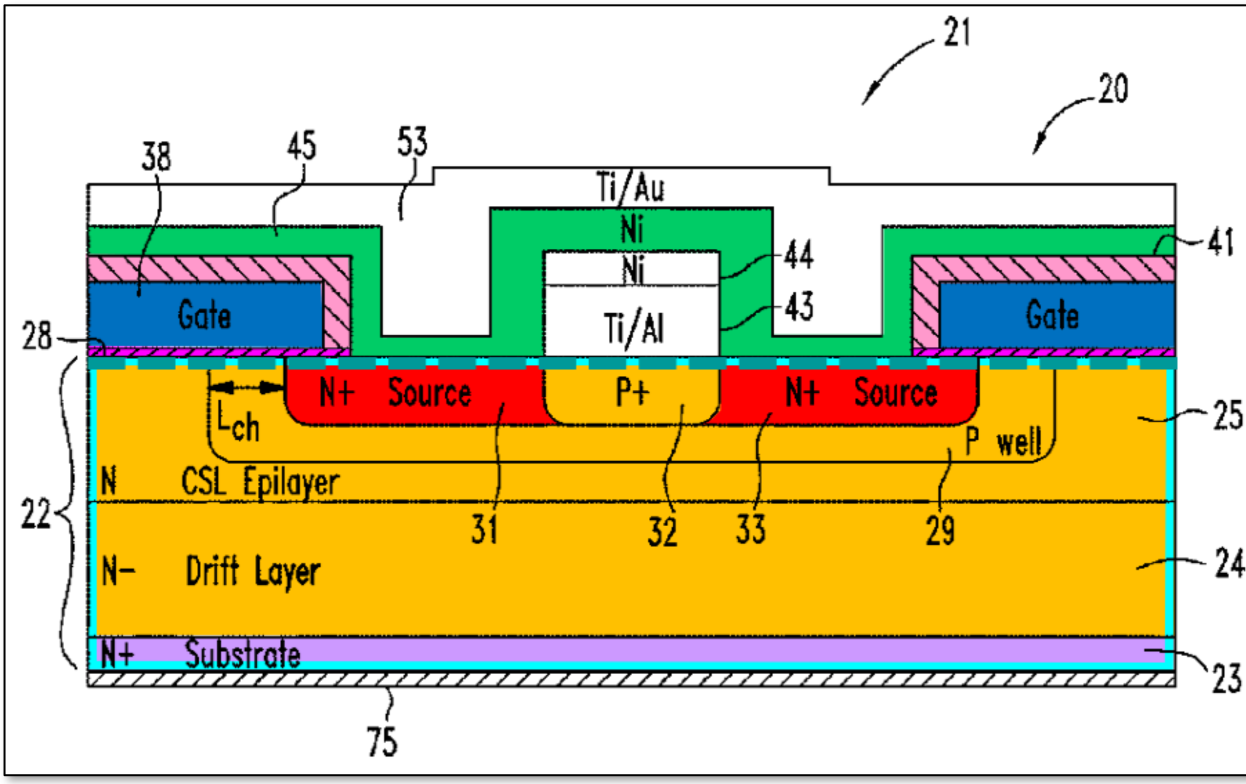


EX1001, FIG. 3 (annotated)

1. Alternative Embodiment Without CSL

The '112 patent describes an alternative embodiment, "wherein there is no separately formed **CSL layer [25]**, and the **drift layer 24** extends all the way to the **top SiC surface 28**." *Id.*, 4:25–26, 4:28–30. This embodiment without **CSL 25** is

illustrated below with the CSL 25 in Figure 3 annotated in the same orange color as **drift layer 24**, such that the **drift layer 24** extends to the **top surface 28**. In this alternative embodiment, the **source regions 31 and 32** are defined in the **drift layer 24**. *Id.*, 10:31–32. EX1028, ¶45.

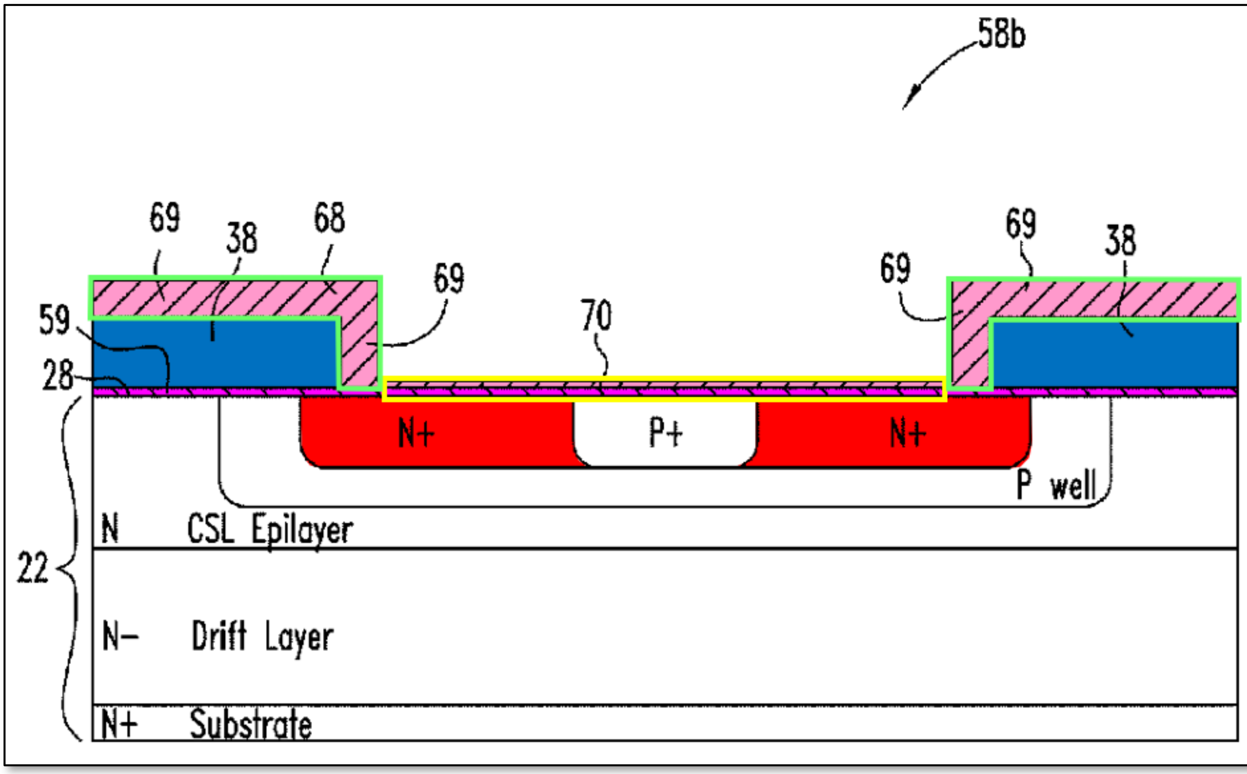


EX1001, FIG. 3 (annotated)

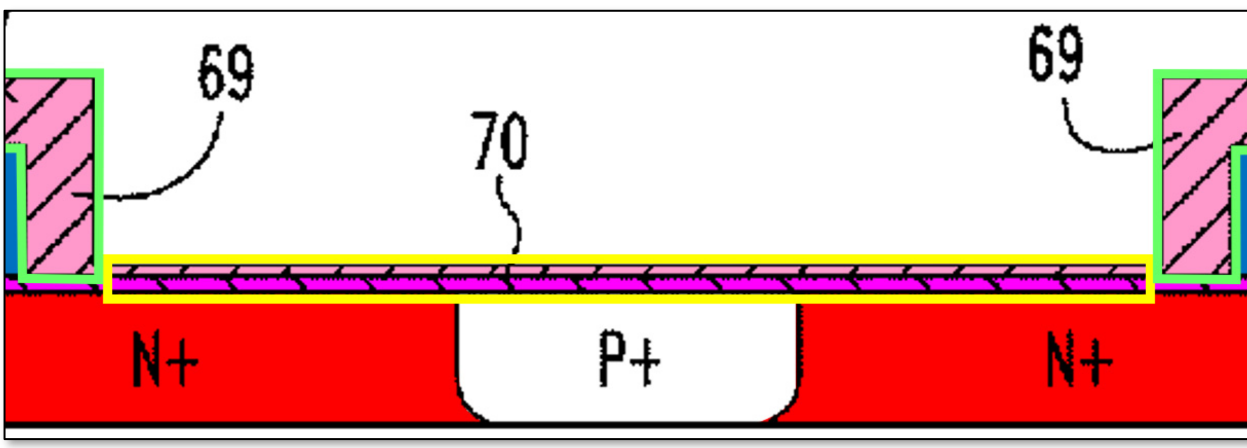
2. Intermediate Semiconductor Products

The ’112 patent describes intermediate semiconductor products at different stages of fabrication. The ’112 patent’s Figure 7 (below) illustrates an intermediate semiconductor product 58b at one particular stage. As the ’112 patent explains, “after the ion etch creates **gates 38**, an **oxidation layer 68** is grown over the entire

upper surface of intermediate semiconductor product 58a . . . to produce intermediate semiconductor product 58b." *Id.*, 6:20–26. "The foregoing oxidation growing step . . . grows oxidation on the **polysilicon gates 38** about ten times faster or more than on the SiC substrate (on which there is already about a 50 nm **oxidation layer 59**)." *Id.*, 6:27–30. "Consequently, **oxidation layer 68** on top and on the sides of each **gate 38** has grown to about 500 nm thick (at 69), while only about 10 nm or less of oxidation are added to upper substrate surface 28 (at 70)." *Id.*, 6:31–34. In other words, the oxidation layer above the **source regions 31 and 32** and between the **gates 38** is the combination of a portion of the **oxidation layer 59** and the portion 70 of the **oxidation layer 68**, and overall is about 60-nm thick. *Id.*, 6:43–45. Below, the **oxidation layer 59** is annotated in magenta and the **oxidation layer 68** in pink. The portion 69 of the **oxidation layer 68** (*i.e.*, on top and on the sides of each **gate 38**) is outlined in light green. Figure 7 represents an intermediate semiconductor product because the combination (outlined in yellow) of the portion of the **oxidation layer 59** and the portion 70 of the **oxidation layer 68** above the **source regions 31 and 32** is etched away prior to the formation of the final MOSFET 21 shown in Figure 3. EX1028, ¶46.



EX1001, FIG. 7 (annotated)



EX1001, FIG. 7 (zoomed, excerpted, and annotated)

As the grounds below demonstrate, the semiconductor structures described and recited in the challenged claims of the ’112 patent—whether final or

intermediate—were well-known in the art before the '112 patent's priority date. EX1028, ¶47.

B. Prosecution History

The '112 patent issued from U.S. Patent Application No. 12/429,176, which was filed on April 23, 2009, claiming priority to U.S. Provisional Application No. 61/047,274 (filed on April 23, 2008).

After a Response to Election/Restriction Requirement and via a Preliminary Amendment, Applicant cancelled original claims 1 and 3 and added new claims 4–18.[3] EX1005, 7–10. The Examiner issued the only Office Action on February 23, 2011, rejecting independent claim 4 over prior art reference Miura and independent claim 2 over prior art reference Kumar in view of Miura and indicating the allowability of independent claim 8. EX1006, 4, 5, 7. The Examiner found claim 8 allowable because the prior art of record "does not teach or suggest the claimed invention having a substrate surface oxidation layer on the upper surface of the substrate body and at least two gates above the substrate surface oxidation layer and a gate oxide layer, thicker than the substrate surface oxidation layer over the tops and sides of each of the gates." *Id.* at 7. The Examiner also indicated that claims 5

[3] Pending independent claims 2, 4, 5, 7, and 8 correspond to issued claims 1, 2, 4, 5, and 6 respectively.

and 7, both of which depend on claim 4, would be allowable if rewritten in independent form. *Id.*

In response, Applicant argued for independent claim 4 that Miura allegedly "discloses only an inter-layer insulation film 7, and nowhere teaches or suggests the composition of such film 7." EX1007 at 11. Therefore, according to Applicant, "Miura does not disclose the composition of the gates or the insulation film, nor does Miura provide any teaching or suggestion what either the gates or insulation film should be made of or what factors would guide such decisions." *Id.* For independent claim 2, Applicant argued that the Examiner failed to make out a *prima facie* case of obviousness and that, "[i]n Fig. 1 of Miura the inter-layer insulation film 7 is depicted as being thicker than the gate oxide films 5a, but Miura nowhere teaches that either of the gate oxide films 5a/5b are to be thicker or thinner than the inter-layer insulation film 7 or that the drawings are intended to be to scale." *Id.*, 12–13. Applicant rewrote claims 5 and 7 in independent form, incorporating all elements of claim 4. *Id.*, 5, 6, 13.

Additionally, Applicant asserted that "applicant's invention provides for a SiC substrate and polysilicon gates because ***growth*** of the oxidation layer on the polysilicon gates occurs considerably faster than on the SiC substrate." *Id.* at 12. The Examiner subsequently issued a Notice of Allowance on June 29, 2011, without providing any reason for allowing claims 2, 4, 5, 7, and 8. EX1008.

As this Petition demonstrates, *Ueno* discloses the allegedly inventive features of the '112 patent, including polysilicon gates and oxide layers formed by the same processes, and the "gate oxide layer, thicker than said first and second oxide layers" recited by claims 2, 4, and 5. EX1028, ¶¶48-52.

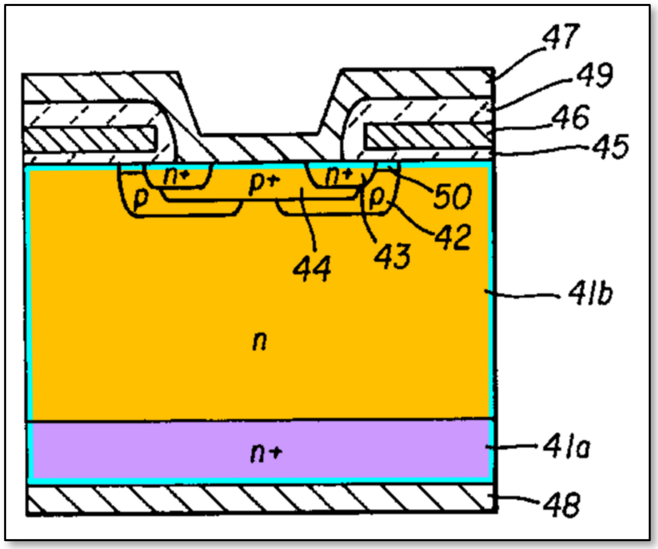
VIII. PRIOR ART PATENTS AND PUBLICATIONS

The following references are pertinent to the grounds of unpatentability:

A. *Ueno*

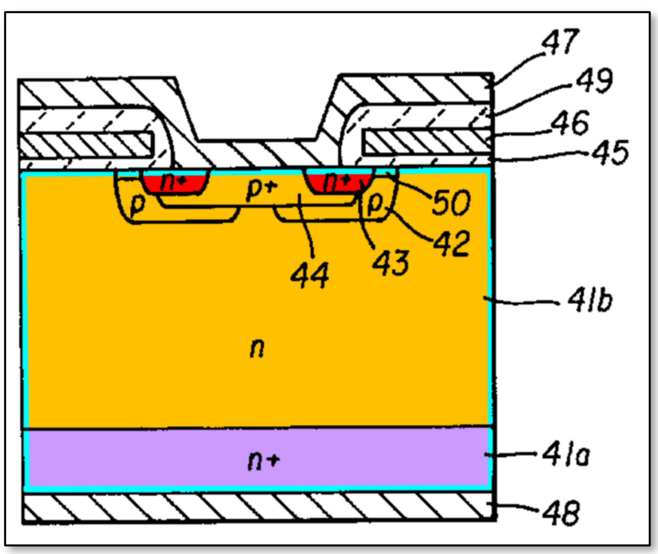
U.S. Patent No. 6,238,980 ("*Ueno*") (EX1003) issued on May 29, 2001. *Ueno* is prior art at least under 35 U.S.C. § 102(b). *Ueno* was of record in the '112 patent's prosecution history, but the Examiner did not describe, address, or apply *Ueno* substantively in rejecting the claims.

Like the '112 patent, *Ueno* relates to SiC vertical power MOSFETs. EX1003, 1:7–14, 4:44–50. *Ueno*'s Figure 1 (below) shows a cross-sectional view of a unit cell of an embodiment of *Ueno*'s MOSFET, which, as explained below, is strikingly similar to the '112 patent's MOSFET. EX1003, 7:31–33, 7:65–67; EX1001, Figure 3. In Figure 1, *Ueno* discloses a **wafer** (cyan below) in which an n **drift layer 41b** (orange) is grown on an "n+ drain layer or **substrate 41a**" (lavender). EX1003, 8:1–13, 8:54–55. EX1028, ¶54.



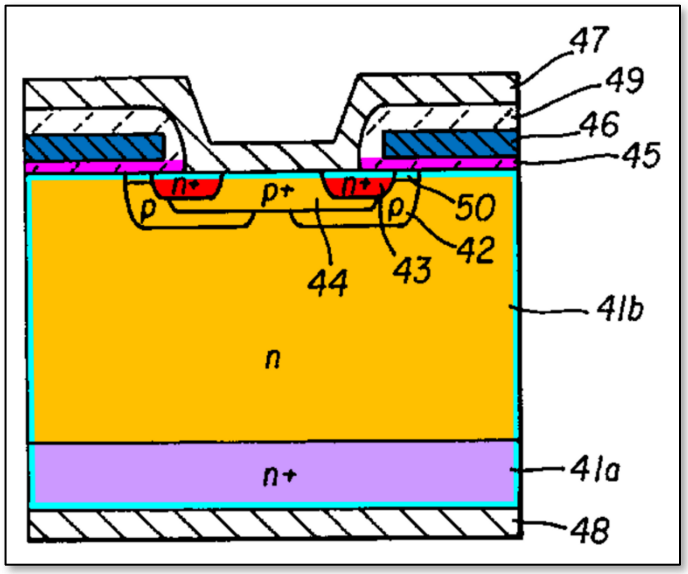
EX1003, FIG. 1 (annotated)

Ueno further discloses that "a p base region 42 is formed in a surface layer of the n **drift layer 41b**, and an n+ **source region 43** is formed within the p base region 42." *Id.*, 8:2–4. As shown in Figure 1, *Ueno*'s MOSFET includes two **source regions 43** (red). EX1028, ¶55.



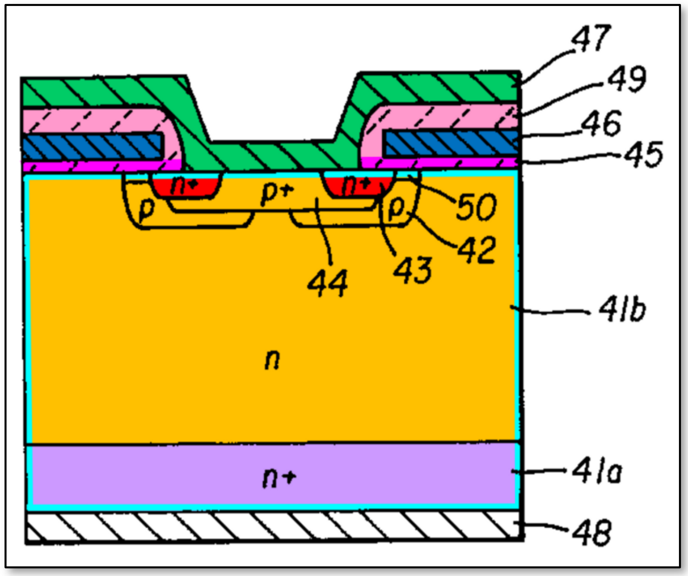
EX1003, FIG. 1 (annotated)

Gates (blue) are formed on **gate oxides** (magenta) over the surface of the n **drift layer 41b**. *Id.*, 8:6–10, 10:42–44, Figures 3c, 3d. EX1028, ¶56.



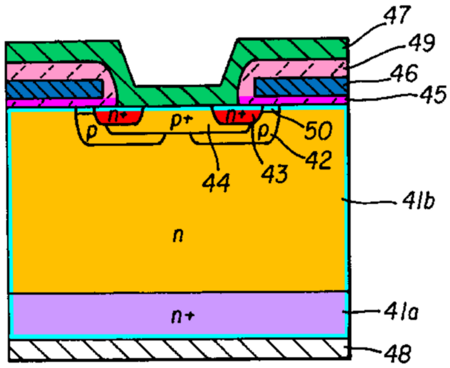
EX1003, FIG. 1 (annotated)

A **source electrode 47** (green) is formed in contact with the n+ **source regions 43**. *Id.*, 8:10–11. An **interlayer insulating film 49** (pink) insulates each **gate** from the **source electrode 47**. *Id.*, 8:13–16. EX1028, ¶57.

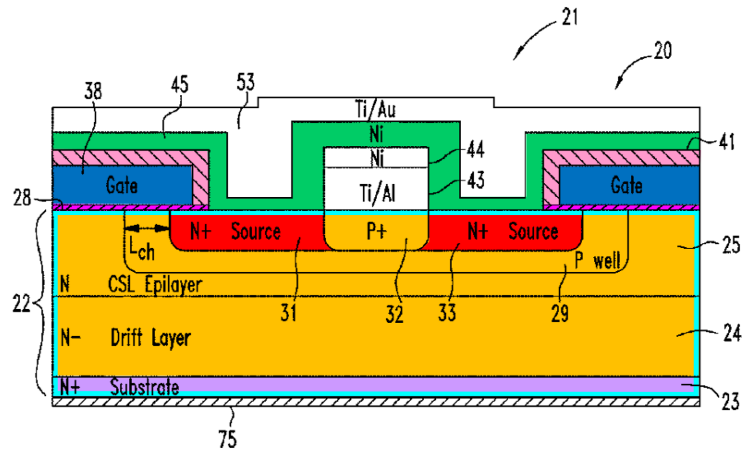


EX1003, FIG. 1 (annotated)

Comparing *Ueno*'s Figure 1 with the '112 patent's alternative MOSFET embodiment (*i.e.*, without the CSL 25) reveals that *Ueno* discloses the same relevant semiconductor structure as the '112 patent. In the '112 patent's MOSFET, the Ti/Al contact metal 43 and the Ni contact metal 44 are added to the basic structure to purportedly improve the quality of the electrical contact to the P+ base 33, but are not relevant to this Petition because they are not recited in any challenged claim of the '112 patent. EX1028, ¶58.



EX1003, FIG. 1 (annotated)

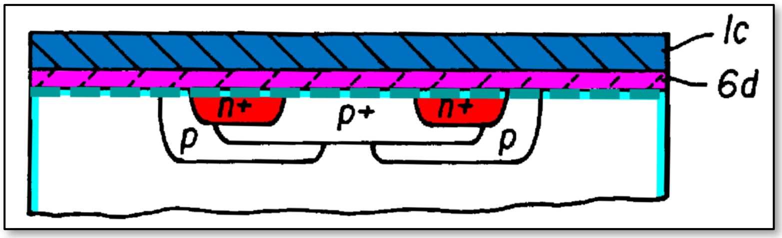


EX1001, FIG. 3 (annotated)

1. Intermediate Structures

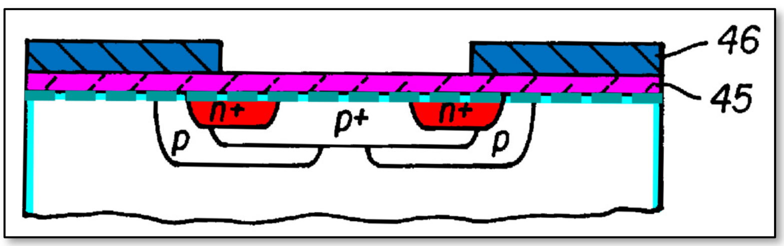
Like the '112 patent, *Ueno* describes and illustrates "cross-sectional views showing the process steps for manufacturing the SiC vertical MOSFET of FIG. 1." EX1003, 7:34–39, Figures 2a–3f. In Figure 3c–3f, *Ueno* steps through the formations of the **gates**, **gate oxides**, and **interlayer insulating film 49**. EX1028, ¶59.

In Figure 3c (below), "an oxide film 6d that . . . provides the gate oxide film 45 is formed by conducting thermal oxidation," followed by deposition of a polysilicon film 1c. EX1003, 10:35–40. Below, the **oxide film 6d** is colored in magenta and the **polysilicon film 1c** in blue. The **oxide film 6d** is formed on an **upper surface** (identified with a dashed teal line) of *Ueno*'s **wafer** and adjacent the **source regions 43**, and the **polysilicon film 1c** is formed on top of the **oxide film 6d**. EX1028, ¶60.



EX1003, FIG. 3c (annotated)

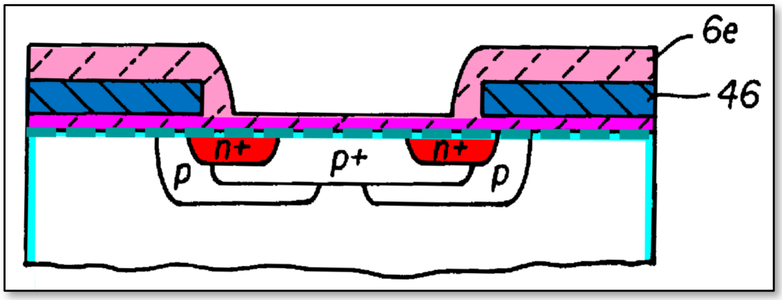
In the next step, shown in Figure 3d, the "**polysilicon film 1c** is patterned by photolithography, to provide the gate electrode layer 46." *Id.*, 10:42–44. The patterning of **polysilicon film 1c** into individual structures 46 forms the polysilicon **gates** on the **gate oxide film 45**. EX1028, ¶61.



EX1003, FIG. 3d (annotated)

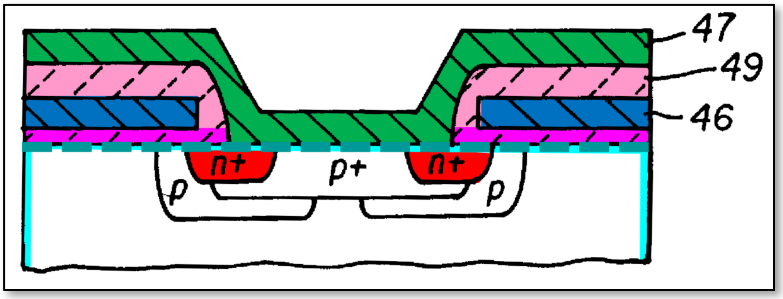
"Then, thermal oxidation is conducted . . . to form an oxide film 6e on the **polysilicon film 1c** and the surface of the SiC substrate," as *Ueno* shows in Figure 3e. *Id.*, 10:43–46. The **oxide film 6e** is colored pink below. During this thermal oxidation process step, the SiC substrate underneath the **gate oxide film 45** oxidizes to form silicon dioxide at a much slower rate than the silicon dioxide that grows from the polysilicon gates. A POSITA would have understood that there is a slight

increase in thickness of the oxide (which includes a portion of **gate oxide film 45**) between the gates and above the **source regions 43**. EX1028, ¶62.



EX1003, FIG. 3e (annotated)

Thereafter, "[t]he entire area of the **oxide film 6e** is subjected to wet etching or dry etching so that only a portion of the **oxide film 6e** that lies on the SiC substrate is removed, thus exposing an electrode contact portion to the outside." *Id.*, 10:48–51. "The oxide film 6e formed on and along the side of the gate electrode layer 46 provides the **interlayer insulating film 49**." *Id.*, 10:59–61. "After forming the contact hole, an aluminum alloy film is deposited, and patterned, as shown in FIG. 3(f), so as to provide the source electrode 47." *Id.*, 10:61–63. *Ueno*'s Figure 3f is below, with the **source electrode 47** colored in green. A POSITA would understand that, to form the contact hole for the **source electrode 47** to contact the **source regions 43**, both the **oxide film 6e** and the portion of the **gate oxide film 45** between the **gates** and above the **source regions 43** get etched away, leaving behind the **interlayer insulating film 49** and the **gate oxides** underneath the **gates**. EX1028, ¶63.

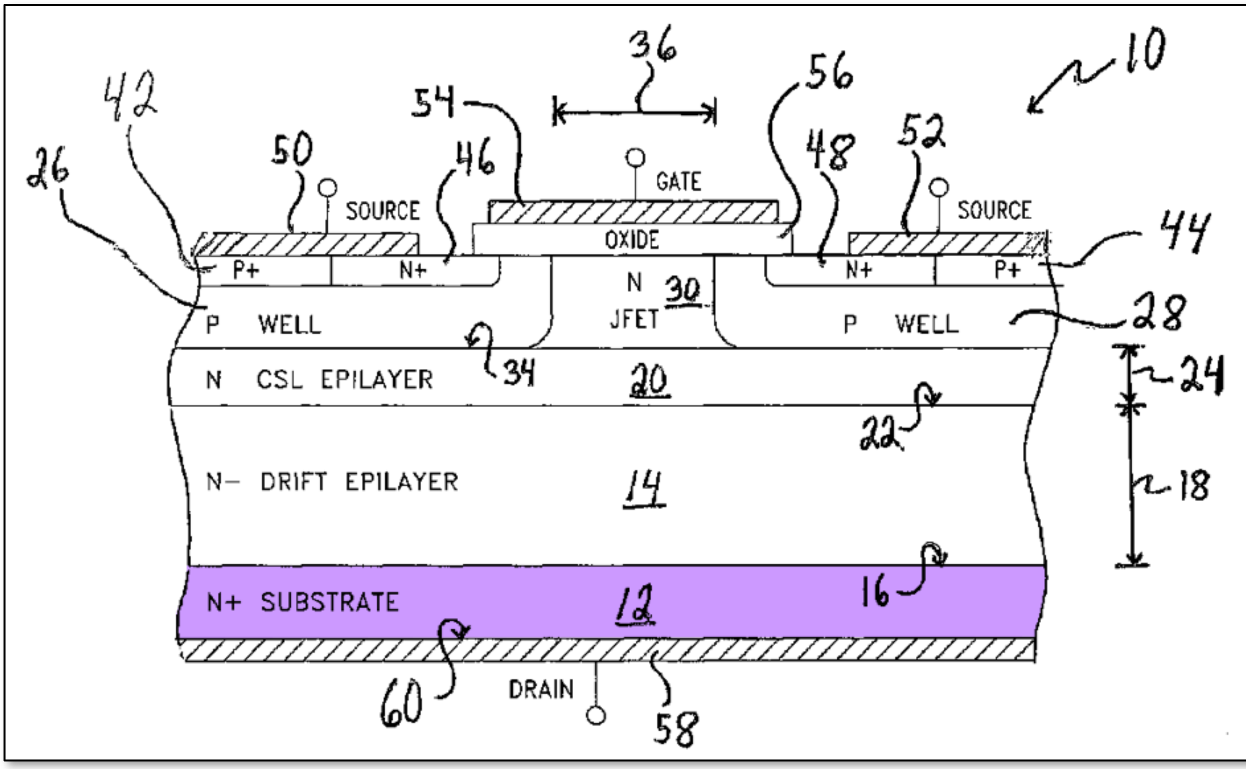


EX1003, FIG. 3f (annotated)

B. *Cooper*

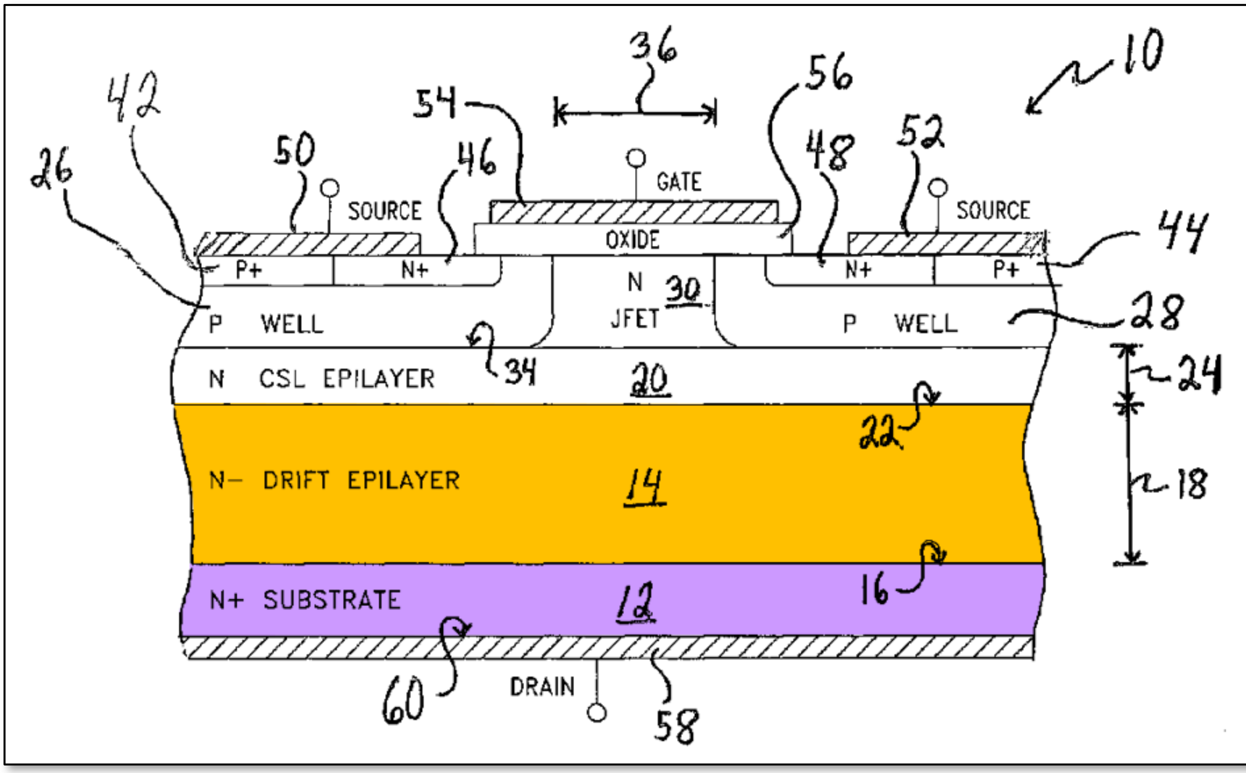
U.S. Patent Application Publication No. 2006/0192256 ("*Cooper*") (EX1026) to the same inventors as the '112 patent—James Cooper and Asmitha Saha—was published on August 31, 2006, more than nineteen months before the claimed priority date of the '112 patent (April 23, 2008). *Cooper* is thus prior art at least under 35 U.S.C. § 102(b). U.S. Patent No. 7,498,633, which issued from the *Cooper* application, was of record in the '112 patent's prosecution history. However, the Examiner did not describe, address, or apply the '633 patent substantively in rejecting the claims.

Like the '112 patent, *Cooper* is directed to semiconductor devices for high-voltage power applications, in particular a "vertical double-implanted metal-oxide semiconductor field-effect transistor." EX1026, ¶¶2, 9, 17, Figure 1. *Cooper* discloses and illustrates in Figure 1 a semiconductor device 10, which includes a **substrate 12** (lavender) that can be formed from silicon-carbide material and doped with N-type impurity to an "N+" concentration. *Id.*, ¶¶12, 17. EX1028, ¶64.



EX1026, FIG. 1 (annotated)

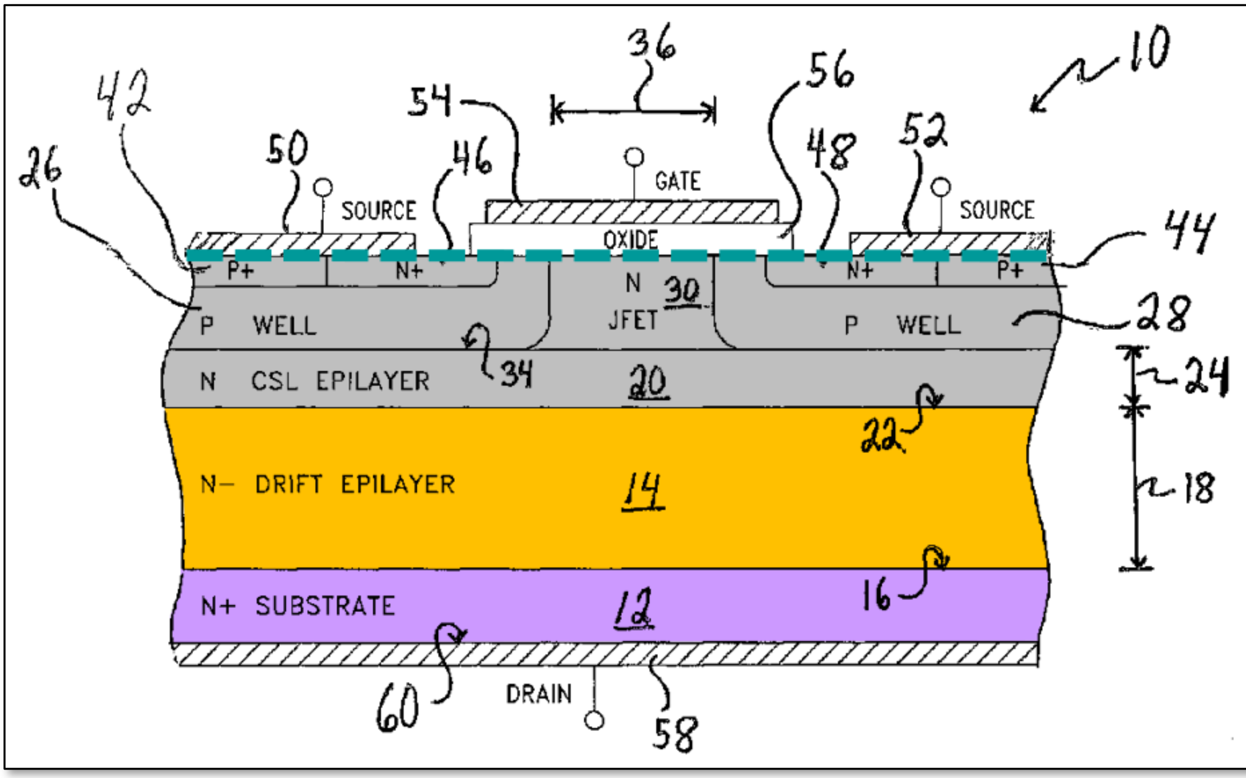
The semiconductor device 10 also includes a **drift layer 14** (orange) formed on a front side 16 of the **substrate 12**. *Id.*, ¶18. The **drift layer 14** may be epitaxially grown and formed of silicon-carbide, and doped with N-type impurities to an "N–" concentration. *Id.*, ¶19. EX1028, ¶65.



EX1026, FIG. 1 (annotated)

The semiconductor device 10 further includes a **current spreading layer (CSL) 20** (grey) formed on a front side of the **drift layer 14**. *Id.*, ¶21. In one embodiment, *Cooper* teaches "growing an extra-thick current spreading layer 20 and forming the 'P' wells 26, 28 using a suitable incorporation process such as an ion implantation process." *Id.*, ¶24. In this embodiment, the **CSL 20** extends to the **top**

surface (identified with a dashed teal line) as shown in *Cooper*'s annotated Figure 1 below.[4] EX1028, ¶66.



EX1026, FIG. 1 (annotated)

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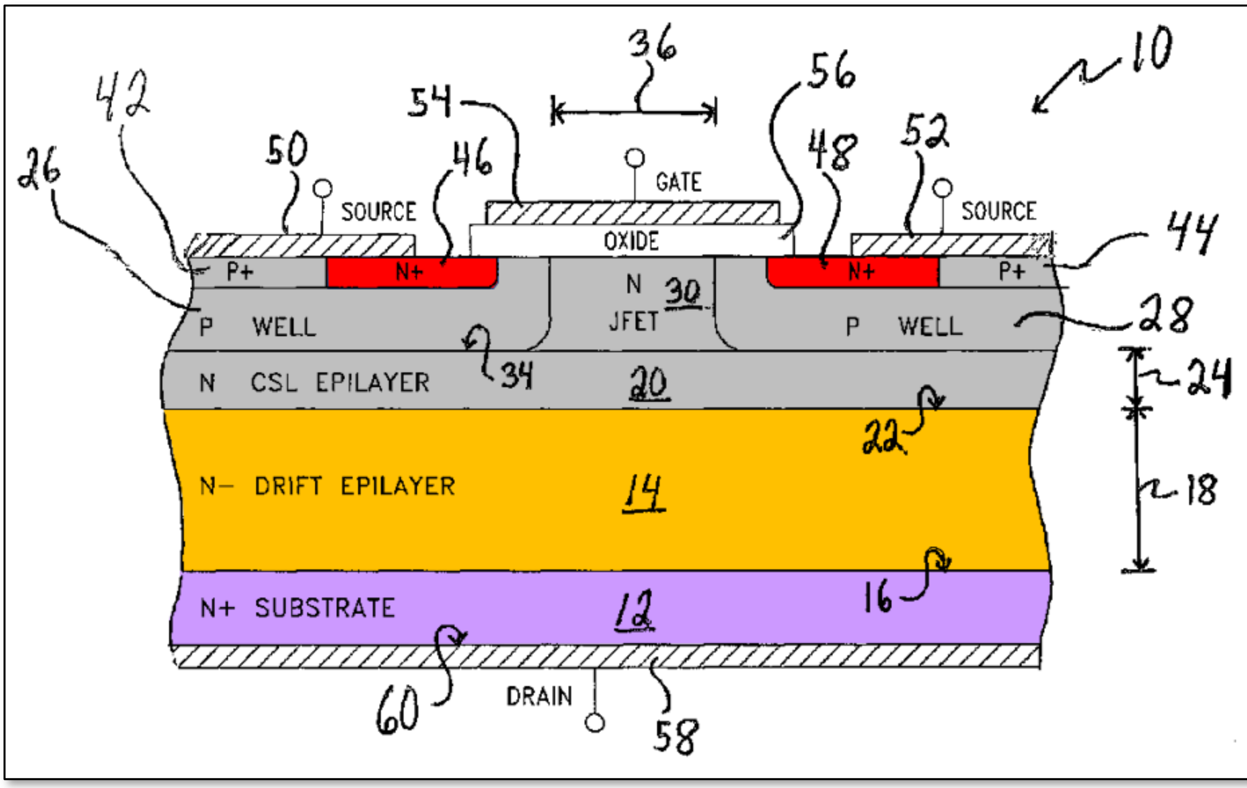
[4] *Cooper* discloses an alternative embodiment, in which "an additional epitaxial layer may be formed on a front side 34 of the current spreading layer 20," and "implanting the wells 26, 28 in the additional epitaxial layer using an ion implantation process." EX1026, ¶25. While this alternative embodiment is discussed in the petition for co-pending IPR2022-00252, it is not relied upon in this Petition. EX1028, ¶67.

Source regions 46, 48 (red) are "defined in the P wells 26 and 28, respectively," and are "doped with N-type impurities to a 'N+' concentration." *Id.*, ¶29. The **source regions 46, 48** are thus defined in the **CSL 20**. EX1028, ¶68.



EX1026, FIG. 1 (annotated)

IX. CLAIM CONSTRUCTION

During IPR, claims are construed according to the "*Phillips* standard." *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc); 83 Fed. Reg. 51341 (Oct. 11, 2018). The Board need only construe the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Sys., Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015); *Nidec Motor Corp. v.*

Zhongshan Broad Ocean Motor Co., 868 F.3d 1013, 1017 (Fed. Cir. 2017). Here, given the close correlation between the asserted prior art and the challenged claims of the '112 patent, the Board need not construe any terms to resolve the underlying controversy, as any reasonable interpretation of those terms consistent with their plain meaning (as would have been understood by a POSITA at the time of the invention, having taken into consideration the language of the claims, the specification, and the prosecution history of record) reads on the prior art.[5]

X. SPECIFIC GROUNDS FOR UNPATENTABILITY

Under 37 C.F.R. § 42.104(b)(4)–(5), the following sections (as confirmed in Dr. Subramanian's declaration, EX1028, ¶¶69–165) detail the grounds of unpatentability, the limitations of challenged claims 2–5, 8, 9, and 13–16 of the '112 patent, and how these claims were obvious in view of, the prior art. EX1028, ¶¶69–165.

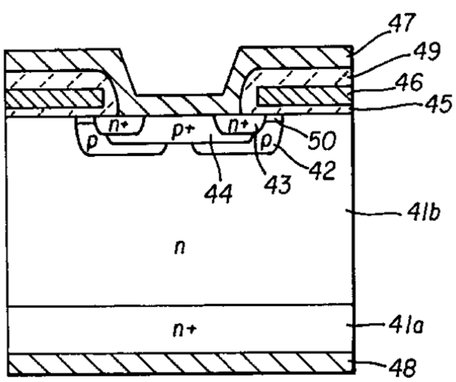
[5] Petitioner reserves all rights to raise claim construction and other arguments in this and other proceedings as relevant and appropriate.

A. Ground I: Claims 2–5, 8, 9, 13, and 14 are Obvious Over *Ueno*

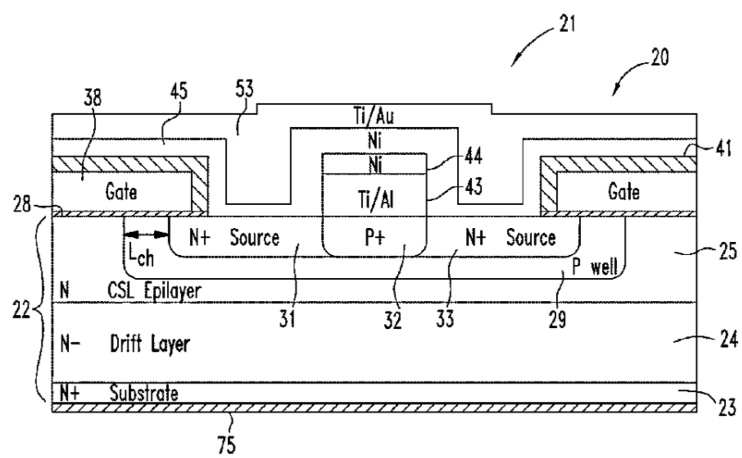
1. Claim 2

a) 2[preamble]: "A silicon carbide MOSFET structure, comprising:"

Regardless of whether the preamble is limiting, *Ueno* discloses it. *Ueno* explicitly discloses that "FIG. 1 is a cross-sectional view showing a part of a **SiC** vertical **MOSFET** . . ." EX1003, 7:31–32. "SiC" is a standard term and chemical abbreviation for referring to silicon carbide. *See, e.g.*, EX1011, 658 ("silicon carbide (SiC)"); EX1012, 956 ("Silicon carbide (SiC)"). *Ueno* uses "SiC" in the conventional way to refer to silicon carbide. EX1003, 1:18 ("Silicon carbide (hereinafter referred to as 'SiC')"). *Ueno*'s Figure 1 is reproduced below for comparison with the '112 patent's Figure 3. EX1028, ¶71.



EX1003, FIG. 1



EX1001, FIG. 3

Further, *Ueno* discloses that its invention relates to "a method for manufacturing silicon carbide MOS semiconductor devices, such as MOS field-effect transistors (hereinafter referred to as '**MOSFET**'), having a MOS type gate

of metal-oxide-semiconductor **structure**, which use **silicon carbide** as a semiconductor material and serve as **power semiconductor devices**." EX1003, 1:7–14. *See also id.*, 3:3–5. Thus, *Ueno*'s MOSFET is "*a silicon carbide power MOSFET structure*." EX1028, ¶72.

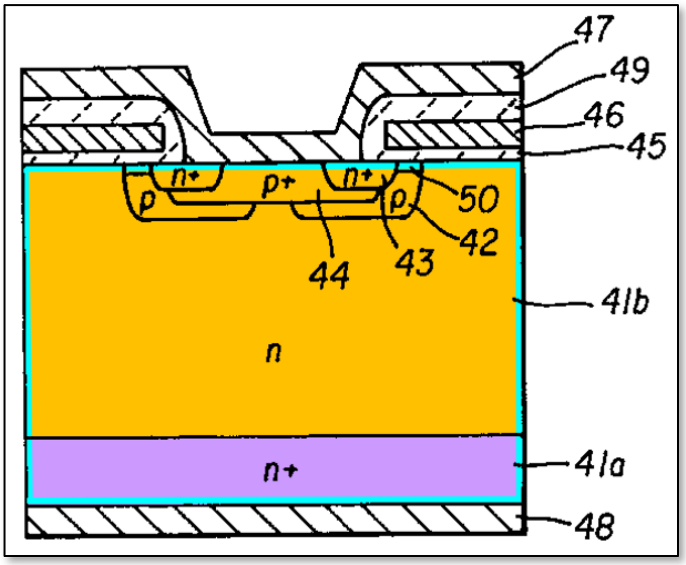
b) 2[a]: "a silicon carbide wafer having a substrate body having a source region formed adjacent an upper surface thereof;"

Ueno discloses element 2[a]. As explained below, *Ueno* discloses a silicon carbide **wafer** having an n **drift layer 41b** grown on **substrate 41a** (collectively a "*substrate body*"). EX1003, 8:1–2, 8:54–55 ("the n drift layer 41b . . . is epitaxially grown on the n+ drain layer 41a"). Moreover, *Ueno* has at least one **source region 43** formed adjacent the substrate body's **upper surface**. *Id.*, 8:3–4 ("n+ source region 43"). EX1028, ¶73.

i. 2[a1]: "a silicon carbide wafer"

Ueno discloses element 2[a1]. *Ueno* explicitly discloses a **wafer** in which an n **drift layer 41b** is grown on an n+ drain **layer 41a**. EX1003, 8:1–2, 8:54–55. *Ueno* uses "drain layer" and "substrate" interchangeably to refer to layer 41a. *Id.*, 8:12–13 ("n+ drain layer or substrate 41a"). *Ueno* also discloses that "the n **drift layer 41b** doped with phosphorous is epitaxially grown on the n+ drain **layer 41a**, to provide a 4H-SiC substrate." *Id.*, 8:54–56. 4H-SiC is a type of ***silicon carbide***.

See id., 7:61–67. *Ueno*'s Figure 1 is below, with the **wafer** in cyan, **substrate 41a** in lavender, and **drift layer 41b** in orange. EX1028, ¶74.



EX1003, FIG. 1 (annotated)

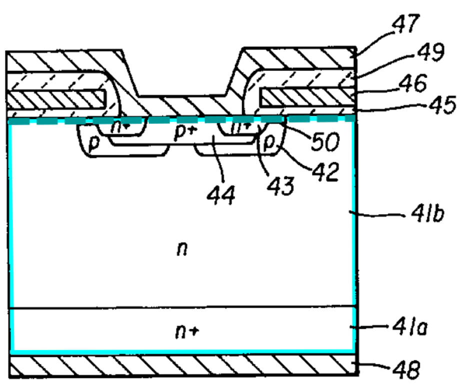
Ueno states that, "[w]hile numerous polytypes of silicon carbide are available, 6H-SiC and 4H-SiC are mainly employed in the following embodiment." EX1003, 7:61–64. A POSITA would have understood this disclosure to mean that both *Ueno*'s **drift layer 41b** and **substrate 41a** are made of silicon carbide. Because *Ueno*'s drift layer and substrate are silicon carbide, it would have been obvious for *Ueno*'s **wafer** to be silicon carbide. In particular, a POSITA would have understood that silicon carbide chips were formed from silicon carbide wafers, *e.g.*, by epitaxially growing layers on the wafer. *See id.*, 5:48–51 ("epitaxially growing a first conductivity type drift layer comprising silicon carbide, on a silicon carbide substrate, to provide a silicon carbide substrate"), 8:54–56 ("the n **drift layer 41b**

doped with phosphorous is epitaxially grown on the n+ drain **layer 41a**, to provide a 4H-SiC substrate"); *see also* EX1021, 284. Indeed, a POSITA would have understood that forming silicon carbide chips, like *Ueno*'s, from silicon carbide wafers was overwhelmingly the most common way of forming such chips. Further, a POSITA would have understood that the most common fabrication technique for silicon carbide chips such as *Ueno*'s would have been to form many such chips simultaneously on a silicon carbide wafer and then saw the wafer into individual chips or dies, just as was commonly done for silicon wafers. *See, e.g.*, EX1023, 6 ("Tens or hundreds of identical chips are fabricated simultaneously on a silicon wafer."); *id.,* 5, Figures 1.3 and 1.5. Accordingly, *Ueno* teaches "*a silicon carbide wafer*." EX1028, ¶75.

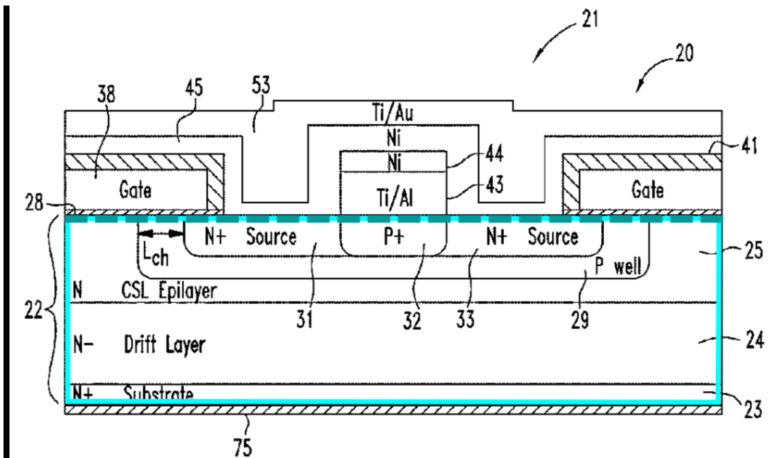
ii. 2[a2]: "having a substrate body"

Ueno discloses element 2[a2]. *Ueno* discloses that, in the **wafer**, "the n drift layer 41b. . . is epitaxially grown on the n+ drain layer 41a." EX1003, 8:1–2, 8:54–55. *Ueno* uses "drain layer" and "substrate" interchangeably to refer to layer 41a. *Id.*, 8:12–13 ("n+ drain layer or substrate 41a"). The '112 patent refers to its substrate body 22 as the collection of its substrate 23 and overlying layers. EX1001, 4:8–11 ("DMOSFET 21 includes a substrate 23 and a number of semiconductor layers and implants formed on or in the substrate 23 up through top surface 28, ***collectively referred to as the substrate body 22***."); *cf.*, EX1019, ¶4 ("the transistor

is formed in a ***body*** 1 ***of semiconductor material comprising*** an N+-type ***substrate*** 2 ***and*** an N−-type ***epitaxial layer*** 3.”). In *Ueno*, the substrate 41a and overlying drift layer 41b form its substrate body. Thus, *Ueno*’s **wafer** has a substrate body. Moreover, *Ueno*’s substrate body has an **upper surface**, as identified with a dashed teal line, below. *Ueno*’s Figure 1 is compared with the ’112 patent’s Figure 3 below. EX1028, ¶76.



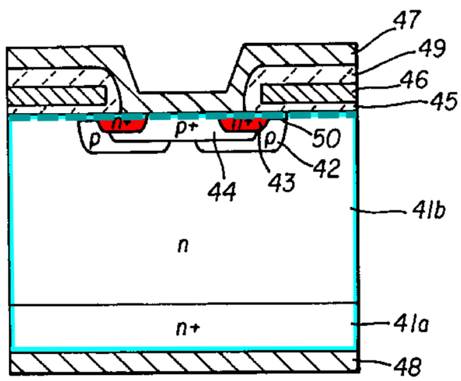
EX1003, FIG. 1 (annotated)



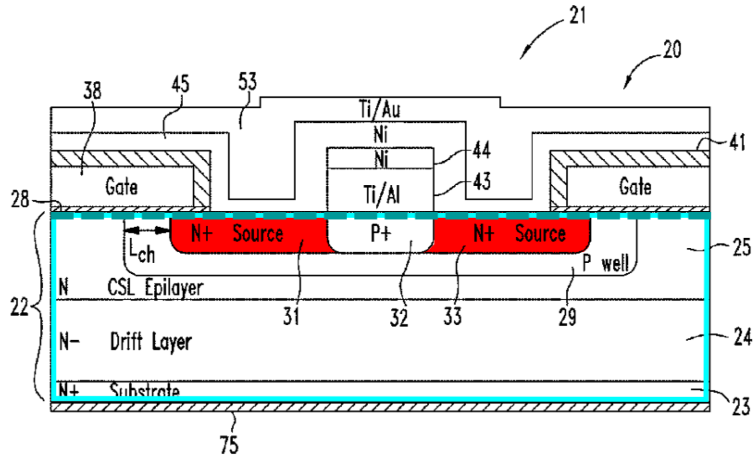
EX1001, FIG. 3 (annotated)

iii. 2[a3]: “having a source region formed adjacent an upper surface thereof”

Ueno discloses element 2[a3]. As explained below, *Ueno*’s Figure 1 shows the **wafer** having two **source regions 43** (red) formed adjacent the **upper surface** of the **wafer**. EX1003, 8:11 (“source region 43”). A side-by-side comparison with the ’112 patent’s Figure 3 shows that, in both *Ueno* and the ’112 patent, the **source regions** are formed adjacent the **upper surface**. EX1028, ¶77.

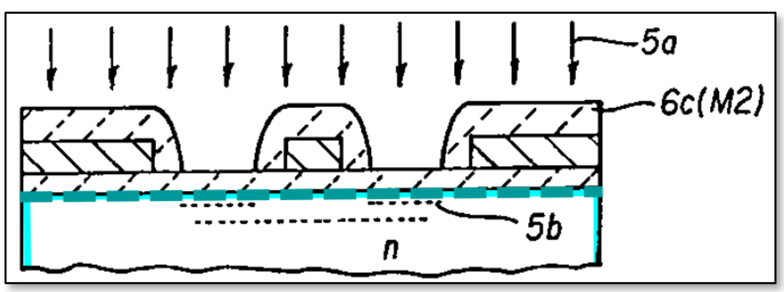


EX1003, FIG. 1 (annotated)



EX1001, FIG. 3 (annotated)

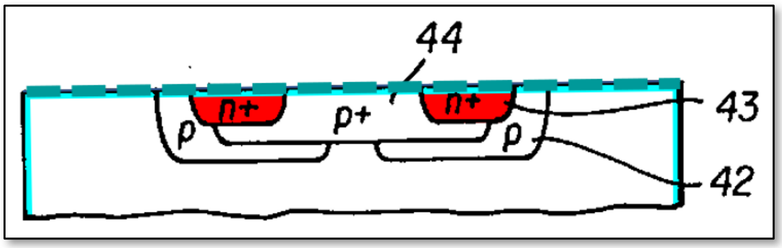
Ueno also discloses the formation of the sources adjacent the upper surface. Specifically, with regard to the process steps for manufacturing the MOSFET of Figure 1, *Ueno* discloses that "nitrogen (N) ions 5a for forming the n+ **source region 43** are implanted" and notes that, in Figure 2g (below), "reference numeral 5b denotes nitrogen [atoms] thus implanted." EX1003, 9:59–62, Figure 2g. As shown in Figure 2g, the nitrogen atoms 5b are adjacent the **upper surface**. EX1028, ¶78.



EX1003, FIG. 2g (annotated)

Furthermore, *Ueno* discloses that, after a heat treatment to activate implanted impurities, the **source regions 43** are formed as in Figure 3b (below). *Id.*, 10:21–

24. Indeed, the **source regions 43** are formed adjacent the **upper surface** and either one corresponds to the "*source region*." EX1028, ¶79.

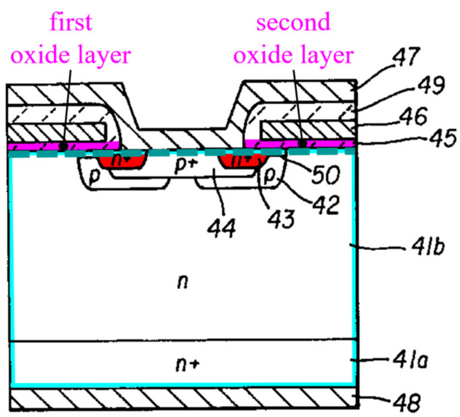


EX1003, FIG. 3b (annotated)

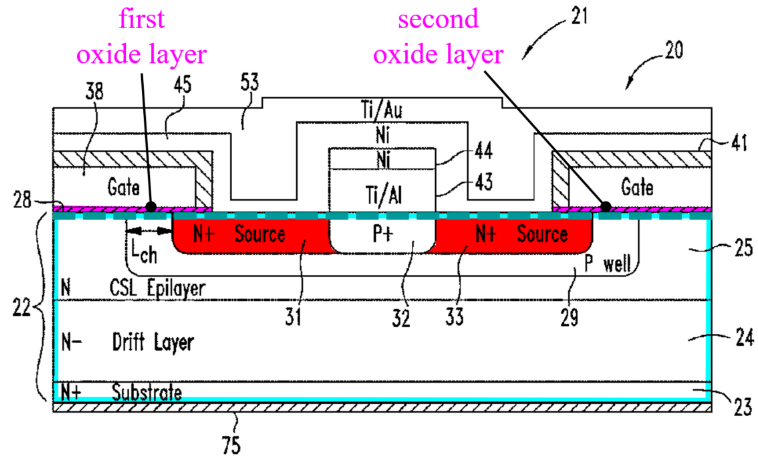
Accordingly, *Ueno* discloses "*having a source region formed adjacent an upper surface thereof*." EX1028, ¶80.

c) 2[b]: "first and second oxide layers on said upper surface adjacent said source region;"

Ueno discloses element 2[b]. For example, *Ueno*'s Figure 1 (below) illustrates, as the oxide layer underneath the left gate, a first **gate oxide** (*i.e.*, "*first oxide layer*") and, as the oxide layer underneath the right gate, a second **gate oxide** (*i.e.*, "*second oxide layer*"). These two **gate oxides** are on the **upper surface** of the **wafer** and each adjacent one of the **source regions 43**. Thus, in both *Ueno* and the '112 patent, there are first and second **oxide layers** on the **upper surface** and adjacent the **source regions**, as shown by the side-by-side comparison below with the '112 patent's Figure 3. EX1028, ¶81.

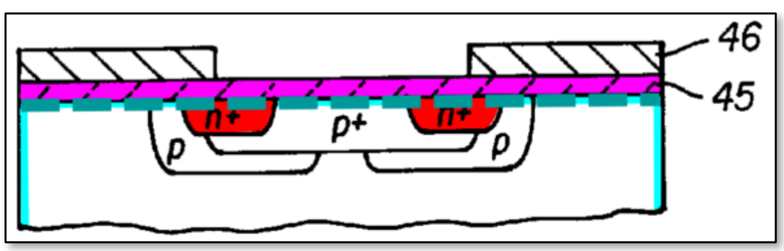


EX1003, FIG. 1 (annotated)



EX1001, FIG. 3 (annotated)

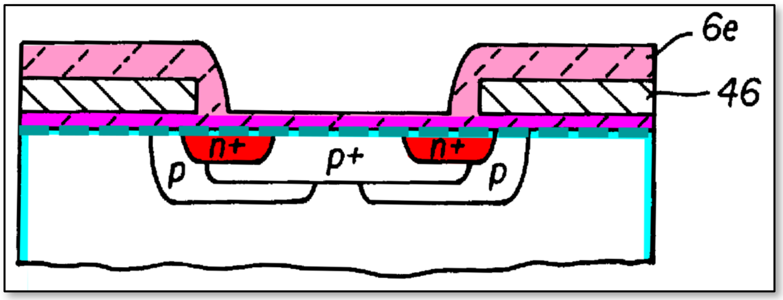
Ueno explains the formation of its two **gate oxides** when describing the process steps for manufacturing its MOSFET of Figure 1. First, "an oxide film 6d . . . provides the **gate oxide film 45**." EX1003, 7:37–39, 10:35–36, Figures 3c and 3d. As shown in Figure 3d, the **gate oxide film 45** is on the **upper surface** of the **wafer**. EX1028, ¶82.



EX1003, FIG. 3d (annotated)

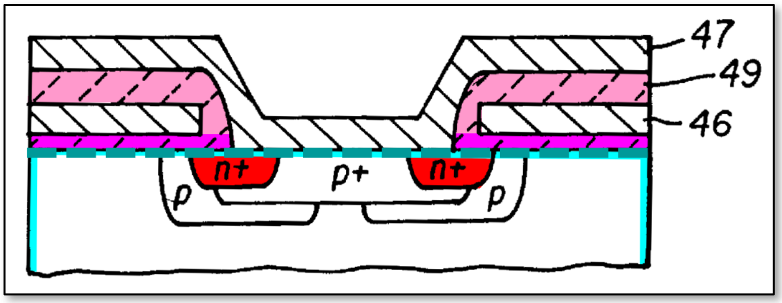
Then, gate electrode layer 46 is formed on top of the **gate oxide film 45** by patterning a polysilicon film 1c. *Id.*, 10:42–44. A thermal oxidation is subsequently conducted "to form an **oxide film 6e** on the polysilicon film 1c and the surface of

the SiC substrate," as *Ueno* illustrates in Figure 3e (below). *Id.*, 10:44–47. EX1028, ¶83.



EX1003, FIG. 3e (annotated)

Thereafter, "[t]he entire area of the **oxide film 6e** is subjected to wet etching or dry etching so that only a portion of the **oxide film 6e** that lies on the SiC substrate is removed, thus exposing an electrode contact portion to the outside." *Id.*, 10:48–51. As shown in *Ueno*'s Figure 3f, a portion of the **gate oxide film 45** between the gate electrode layer 46 and above the **source regions 43** is also etched away during the same process, leaving behind the two **gate oxides** (*i.e.*, "*first and second oxide layers*")—one underneath the left gate and the other underneath the right gate—on the **upper surface** and adjacent the **source regions 43**. *See* Section VIII.A.1. EX1028, ¶84.

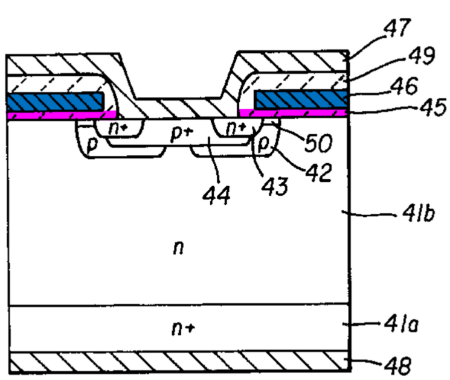


EX1003, FIG. 3f (annotated)

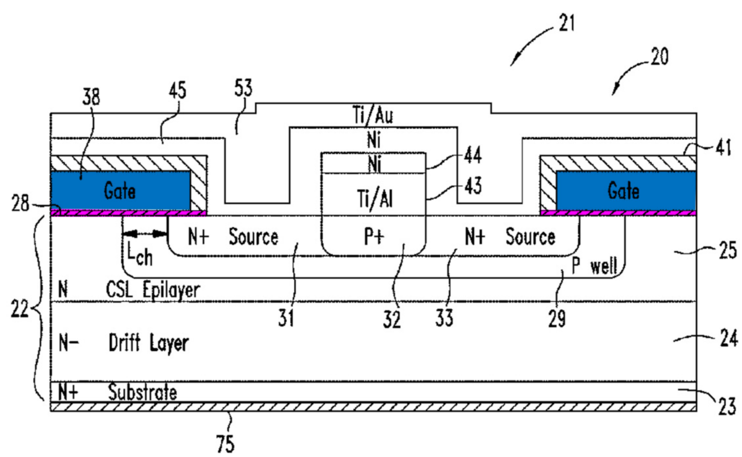
Therefore, *Ueno* discloses element 2[b]. EX1028, ¶85.

d) 2[c]: "a polysilicon gate above each of said first and second oxide layers;"

Ueno discloses element 2[c]. As discussed for element 2[b], *Ueno*'s **gate oxides** correspond to the "*first and second oxide layers*." Moreover, *Ueno*'s Figure 1 (alongside the '112 patent's Figure 3 for comparison) shows a **gate** above each of the **gate oxides**. EX1028, ¶86.



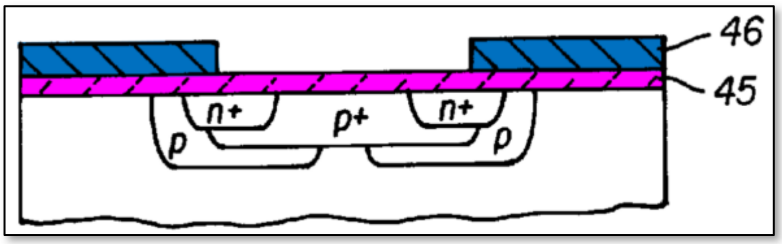
EX1003, FIG. 1 (annotated)



EX1001, FIG. 3 (annotated)

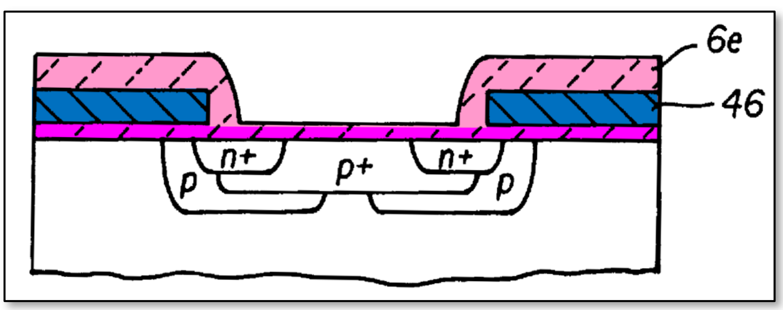
In describing the formation of the two **gate oxides**, *Ueno* also explains the formation of a **gate** on each of the two **gate oxides** when describing the process steps

for manufacturing the MOSFET of Figure 1, a polysilicon film 1c is deposited on the **gate oxide film 45** and patterned to provide the gate electrode layer 46, forming two **gates**, one of the left and the other on the right. EX1003, 7:37–39, 10:39–44, Figures 3c, 3d. *Ueno*'s Figure 3d shows the two **gates** above the **gate oxide film 45**. EX1028, ¶87.



EX1003, FIG. 3d (annotated)

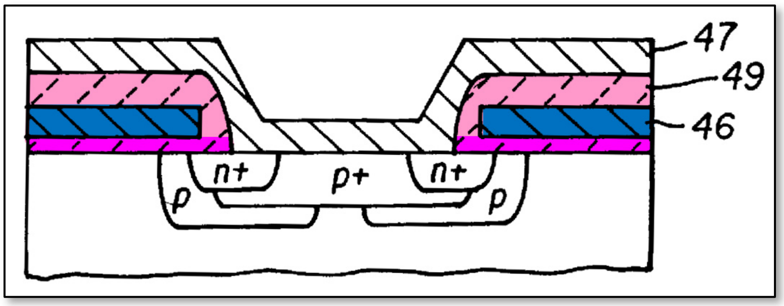
Then, thermal oxidation forms an **oxide film 6e** over the **gates** and the surface of the SiC substrate, as *Ueno* illustrates in Figure 3e (below). *Id.*, 10:43–46. EX1028, ¶88.



EX1003, FIG. 3e (annotated)

Subsequently, the **oxide film 6e** is subjected to etching to expose an electrode contact portion. *Id.*, 10:48–51. During the same etching process, as can be seen in

Ueno's Figure 3f (below), a portion of the **gate oxide film 45** between the two **gates** gets etched away, leaving behind the two **gate oxides**. As a result, a **gate** remains above each of the two **gate oxides**. EX1028, ¶89.



EX1003, FIG. 3f (annotated)

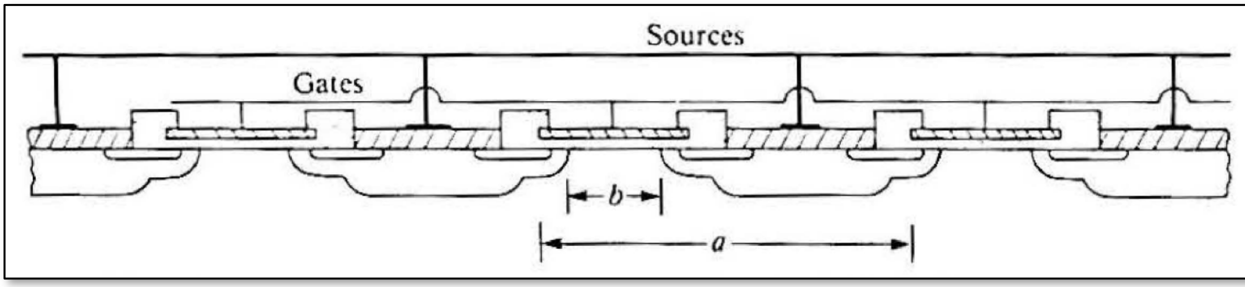
Therefore, *Ueno* discloses element 2[c]. EX1028, ¶90.

e) 2[d]: "a gate oxide layer, thicker than said first and second oxide layers beneath said gates, over each of said gates and the sides thereof; and"

Ueno renders obvious element 2[d]. As discussed for elements 2[b] and 2[c], *Ueno* discloses "*first and second oxide layers,*" "*a polysilicon gate above each of said first and second oxide layers*," and "*said first and second oxide layers beneath said gates*." As explained below, *Ueno* explicitly discloses an oxide layer over the top and a side of each of the **gates** and thicker than the **gate oxides**. Moreover, a POSITA would have recognized that each of the **gates** has a second side that would also be covered by the thicker oxide layer. EX1028, ¶91.

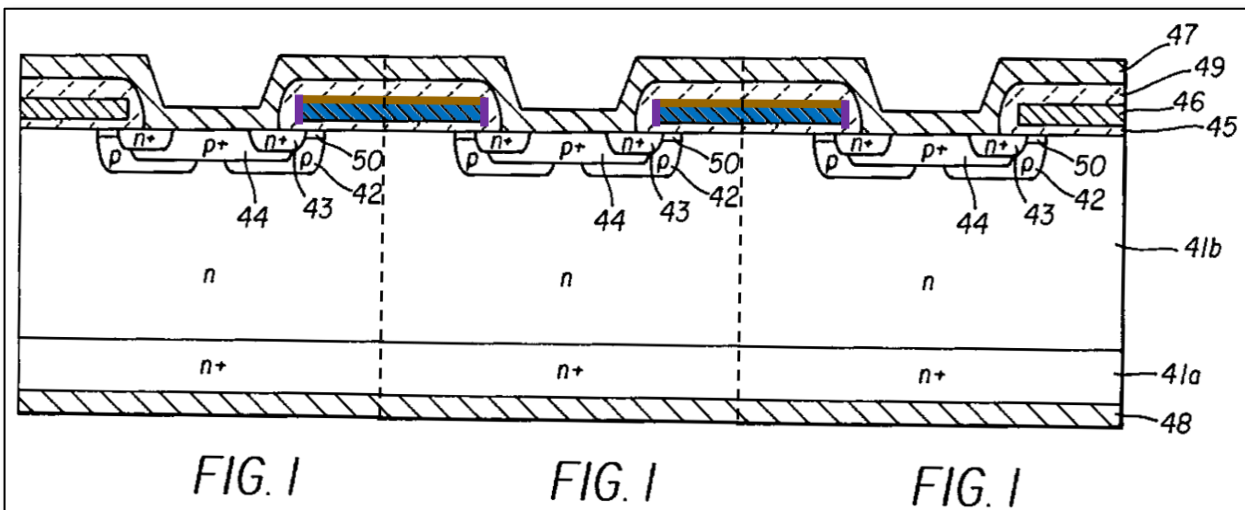
i. "said gates and the sides thereof"

A POSITA would have recognized that, in *Ueno*, each **gate** would have had two sides. *Ueno* discloses that "FIG. 1 is a cross-sectional view of a unit cell of SiC vertical MOSFET according to one preferred embodiment of the present invention." EX1003, 7:65–67. *Ueno* also discloses that "[t]he pitch of unit cells as shown in FIG. 1 is about 25 µm." EX1003, 8:32–33. A POSITA would have understood *Ueno*'s disclosure that Figure 1 is a "unit cell" and the "pitch of the unit cells" to mean that multiple such unit cells are laid out next to each other spaced apart by the pitch of 25 µm. For example, as discussed in Section VI.C above, *Grant* explains this well-known concept of pitch, stating that "VDMOS FET gates may be laid out as linear arrays, interdigitated with the source, as shown in Figure 3.9*a* . . . where *a* is the pitch of the array." EX1009, 455, Figure 3.9a. *Cf.* EX1001, 4:35–38 ("It should be understood that the semiconductor device (MOSFET 21) of FIG. 3 may be a single 'transistor cell' and that a completely fabricated transistor device may include any number of such semiconductor devices or cells."). An excerpt of *Grant*'s Figure 3.9*a* is reproduced below, illustrating the pitch *a.* EX1009, 70–73, Figure 3.9; *see also id.* at 16, Figure 1.13. EX1028, ¶92.



EX1009, Figure 3.9*a* (excerpted)

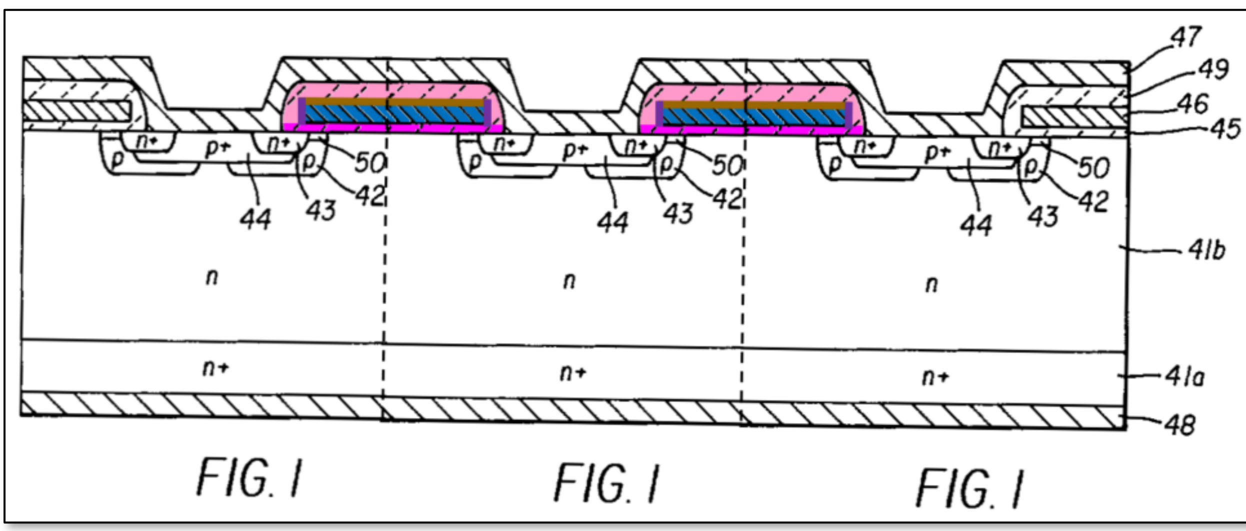
Multiple copies of *Ueno*'s unit cell of Figure 1 are depicted below, side-by-side, per *Ueno*'s teaching of "unit cell" and "pitch of the unit cells" as would be understood by a POSITA and as illustrated and taught by *Grant*. *Ueno* explicitly discloses that each of its two **gates** in Figure 1 has a **top** (outlined in brown). While *Ueno* does not explicitly show both ends of the **gates**, a POSITA would have recognized, at least in view of *Ueno*'s teachings of unit cells and pitch, that each **gate** would have had two **sides** (outlined in purple). EX1028, ¶93.



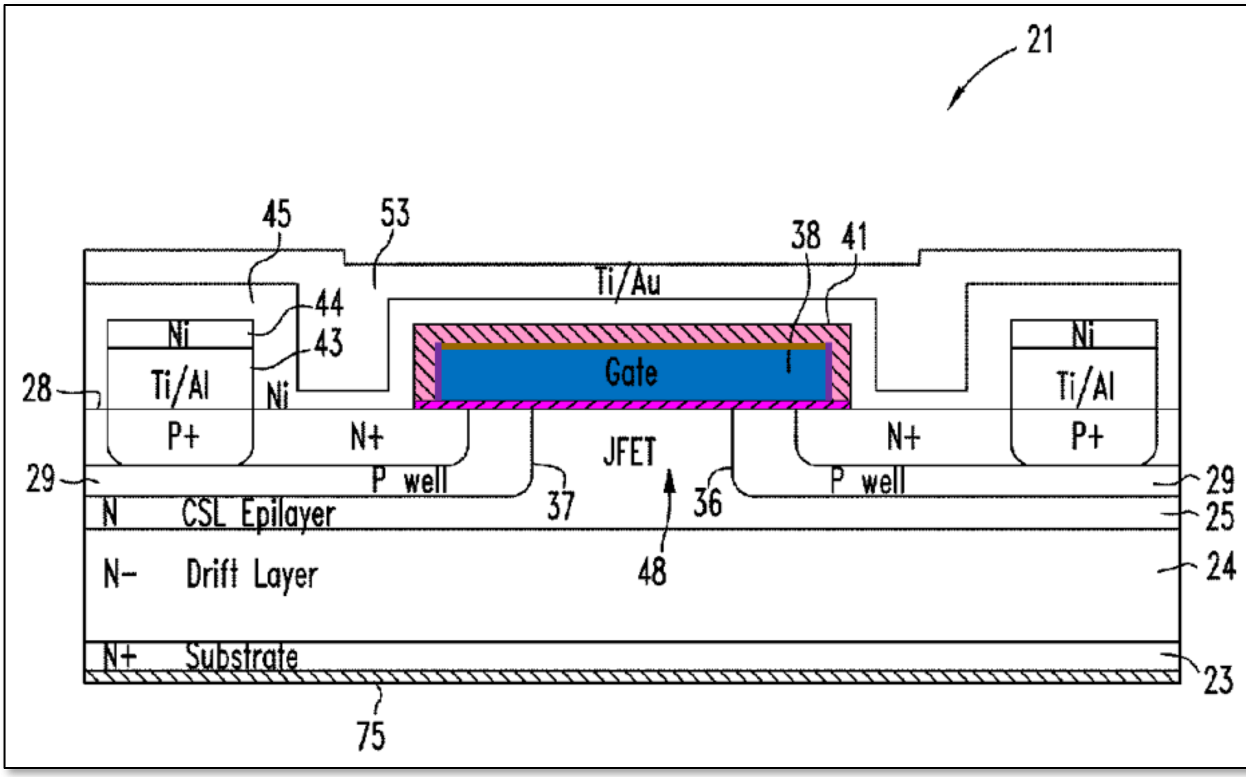
EX1003, FIG. 1 (replicated and annotated)

ii. *"a gate oxide layer . . . over each of said gates and the sides thereof"*

Ueno discloses that, after "the oxide film 6e is subjected to wet etching or dry etching," "[t]he oxide film 6e formed ***on and along the side*** of the gate electrode layer 46 provides the interlayer insulating film 49." EX1003, 7:37–39, 10:48–61, Figures 3e and 3f. A POSITA would have understood that the **interlayer insulating film 49** (pink) would have been formed over the **tops** and the **sides** of the **gates** as illustrated in *Ueno*'s replicated and annotated Figure 1 below, similar to how the **oxide layer** is formed over the **top** and the **sides** of each **gate 38** as illustrated in the '112 patent's annotated Figure 4 below. Thus, *Ueno*'s **interlayer insulating film 49** corresponds to the "*gate oxide layer*." EX1028, ¶94.



EX1003, FIG. 1 (replicated and annotated)

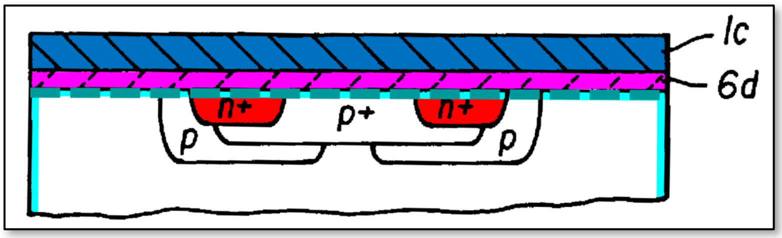


EX1001, FIG. 4 (annotated)

iii. "gate oxide layer, thicker than said first and second oxide layers"

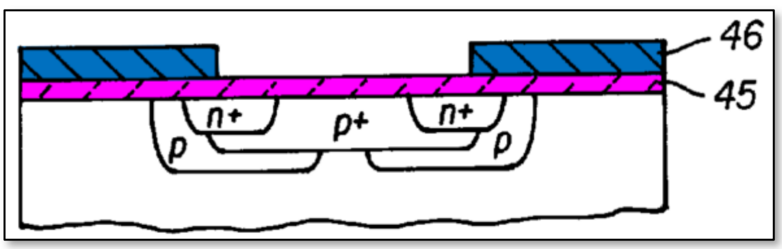
Ueno discloses that its **interlayer insulating film 49** (*i.e.*, the "*gate oxide layer*") is thicker than its two **gate oxides** (*i.e.*, "*first and second oxide layers*"). *Ueno* describes the formation of its **interlayer insulating film 49** and **gate oxides** as follows. First, as shown in *Ueno*'s Figure 3c, "an **oxide film 6d** that has a thickness of 30 nm and provides the gate oxide film 45 is formed by conducting thermal oxidation at 1100°C. for five hours by a pyrogenic method." EX1003, 10:35–38. This is like how the '112 patent grows "the 50 nm thick silicon lower gate oxide layer 59 on top of the entire surface 28 of the SiC substrate body 22 by

thermal oxidation in a pyrogenic oxidation system at 1150° C. for 2.5 hours." EX1001, 5:48–51. Thereafter, in *Ueno*, a "**polysilicon film 1c** having a thickness of 1 µm is deposited" over the **oxide film 6d**. *Id.*, 10:38–40. EX1028, ¶95.



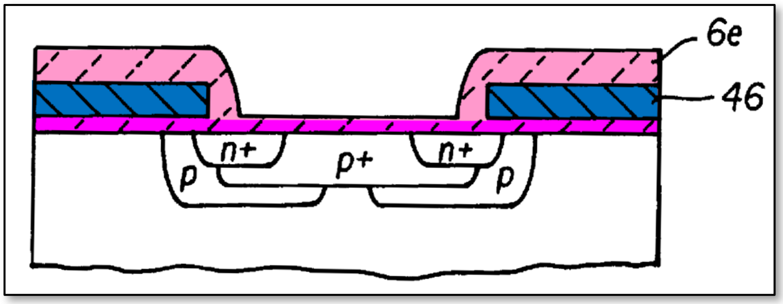
EX1003, FIG. 3c (annotated)

Then, the **polysilicon film 1c** is patterned to provide the gate electrode layer 46, forming the **gates**. EX1003, 7:37–39, 10:39–44, Figures 3c, 3d. *Ueno*'s Figure 3d shows the two **gates** above the **gate oxide film 45**. EX1028, ¶96.



EX1003, FIG. 3d (annotated)

Another thermal oxidation (at 1100°C. for five hours by a pyrogenic method) forms an **oxide film 6e** over the **gates** and the surface of the SiC substrate, as *Ueno* illustrates in Figure 3e. *Id.*, 10:43–46. EX1028, ¶97.

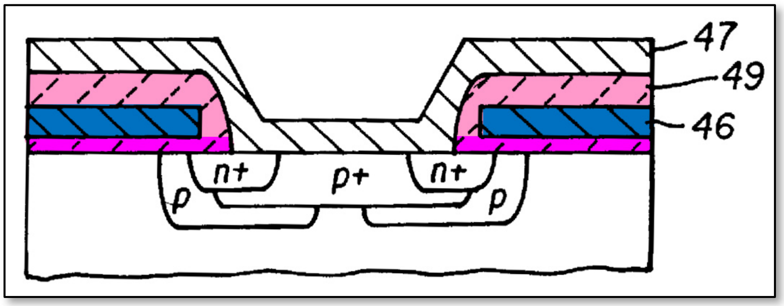


EX1003, FIG. 3e (annotated)

A POSITA would have understood that subjecting the polysilicon gate electrode layer 46 to thermal oxidation would mean that the **oxide film 6e** is grown by oxidation of the polysilicon gate electrode layer 46 and the surface of the SiC substrate between the gates, rather than deposited. *See id.*, Figure 3e. This is also how the '112 patent discloses forming an oxidation layer 68 during an intermediate step in the fabrication of the MOSFET 21. EX1001, 6:20–26 ("an oxidation layer 68 is grown over the entire upper surface of intermediate semiconductor product 58a [by the step of]: Dry oxidation for 6 hrs. at 1000 C …"); *see also id.*, Figure 7. EX1028, ¶98.

According to *Ueno*, the **oxide film 6e** is then subjected to etching such that "[t]he polysilicon film 1c remains covered by the thick **oxide film 6e**." EX1003, 10:48–52. "The **oxide film 6e** formed on and along the side of the gate electrode layer 46 provides the **interlayer insulating film 49**," as can be seen both the intermediate structure shown in Figure 3e above and in the final structure shown in Figure 3f (below). *Id.*, 10:59–61. As shown in Figure 3f, a portion of the **gate oxide**

film 45 between the **gates** gets etched away during the same etching process, leaving behind the two **gate oxides** underneath the two **gates**. EX1028, ¶99.



EX1003, FIG. 3f (annotated)

Further, the **interlayer insulating film 49** is thicker than the two **gate oxides**. *Ueno* states that the "**oxide film 6d** . . . has a thickness of 30 nm" and that the **oxide film 6d** "provides the gate oxide film 45." *Id.*, 10:35–36. *Ueno* also states that "the thickness of the **interlayer insulating film 49** is ***2 µm***." *Id.*, 8:31–32.[6] Converting units, 30 nm is equal to 0.03 µm. 2 µm (two microns) is ***sixty-six times*** thicker than 30 nm (thirty nanometers) (*i.e.*, 2 ÷ 0.03 ≈ 66). Therefore, the **interlayer insulating film 49** (*i.e.*, "*gate oxide layer*") is thicker than the two **gate oxides** (*i.e.*, "*said first and second oxide layers*"). EX1028, ¶100.

Therefore, *Ueno* renders obvious element 2[d]. *Id.*, ¶101.

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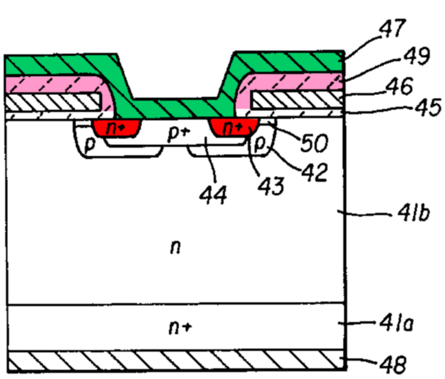
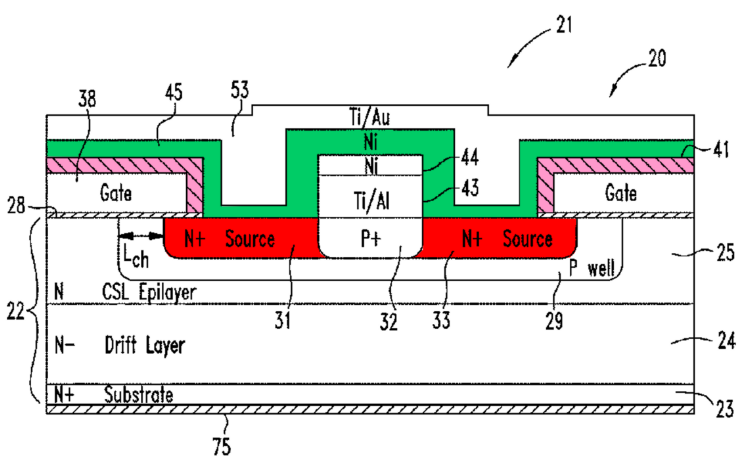
[6] *Ueno* also states that "[t]he thickness of the gate oxide film 75 [*sic*] is 50 nm. EX1003, 8:29–30. Whether the gate oxide film 45 is 30 nm or 50 nm thick, it is clearly much thinner than the 2-µm interlayer insulating film 49. EX1028, ¶100.

f) 2[e]: "a metal or oxide layer over said source region, extending between adjacent gate oxide layers."

Ueno discloses element 2[e]. Indeed, *Ueno* discloses each of a "*metal…layer*" and "*oxide layer*" formed "*over said source region...*". First, *Ueno* discloses that a **source electrode 47** (green below) is formed to be in contact with the n+ **source region 43** (*i.e.*, "*source region*"). EX1003, 8:10–11 ("A source electrode 47 is formed in contact with both the n+ source region 43 and the p+ well region 44 . . ."). *Ueno* explains that "an ***aluminum alloy*** film is deposited, and patterned, as shown in FIG. 3(f), so as to provide the **source electrode 47** . . ." *Id.*, 10: 62–63. Further, as can be seen in *Ueno*'s Figure 1 below (alongside the '112 patent's Figure 3 for comparison), the **source electrode 47** extends between adjacent **interlayer insulating film 49** (*i.e.*, "*gate oxide layer*"). Thus, *Ueno*'s **source electrode 47** is "*a metal layer over said source region, extending between adjacent gate oxide layers*." EX1028, ¶102.

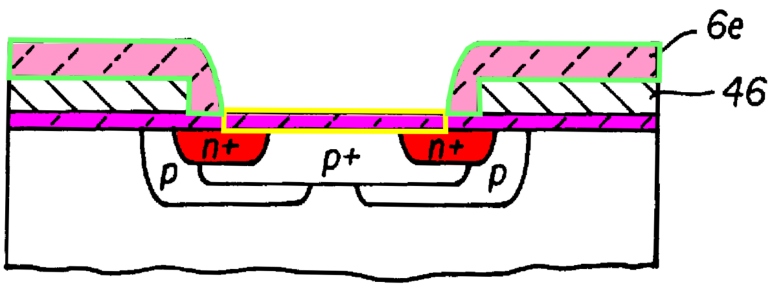


EX1003, FIG. 1 (annotated)

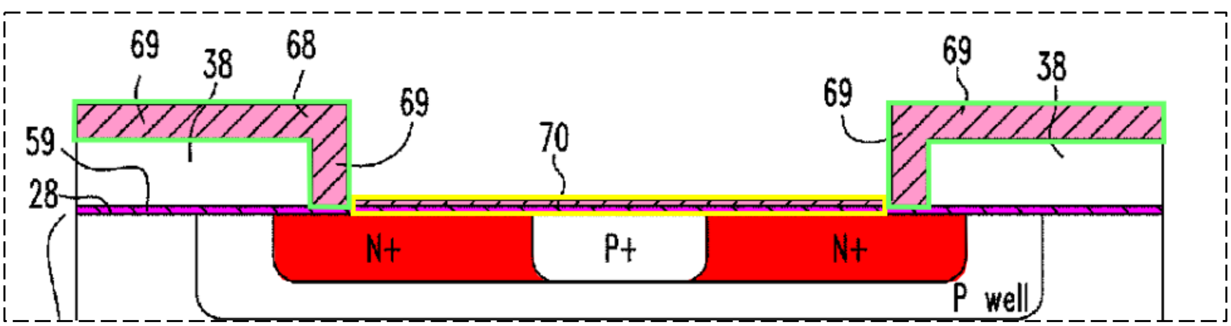


EX1001, FIG. 3 (annotated)

Second, and just like shown in the '112 patent's Figure 7, *Ueno* also discloses an intermediate MOSFET structure with an **oxide layer** (outlined in yellow) extending between portions (outlined in light green) of the oxide film 6e over the sides and on top of the gates that correspond to the **interlayer insulating film 49** (*i.e.*, "*gate oxide layer*") in *Ueno*'s Figures 1 and 3f. Thus, *Ueno* also discloses "*an oxide layer over said source region, extending between adjacent gate oxide layers*." EX1028, ¶103.



EX1003, FIG. 3e (annotated)



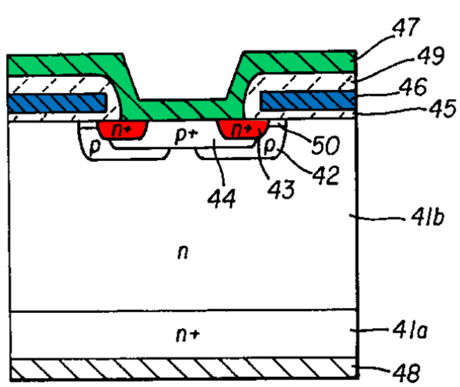
EX1001, FIG. 7 (excerpted and annotated)

Therefore, *Ueno* renders obvious claim 2. EX1028, ¶104.

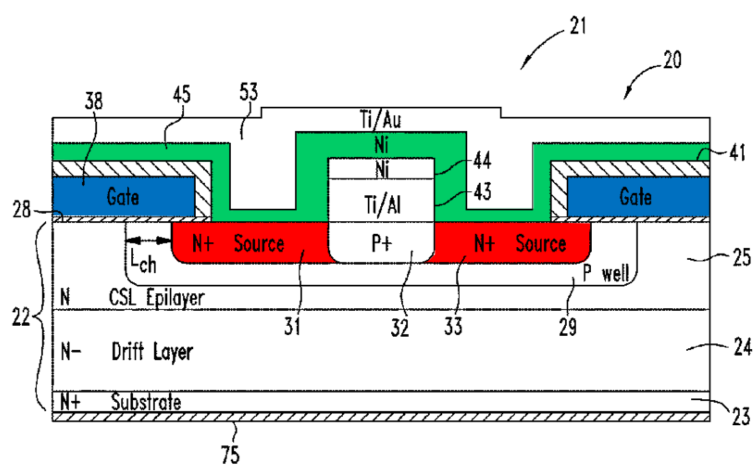
2. Claim 3

> ***"The silicon carbide MOSFET structure of claim 2, wherein said layer over said source region is a conformal layer of metal extending laterally across said gates and said source region."***

Ueno renders obvious claim 2, as discussed above. *Ueno* discloses the additional limitation of claim 3. As discussed for element 2[e], *Ueno*'s **source electrode 47** corresponds to "*a metal layer over said source region*." Moreover, as shown in *Ueno*'s annotated Figure 1 below, the **source electrode 47** conformally and laterally extends laterally across the gate electrode layer 46 that forms the **gates** (*i.e.*, "*said gates*") and each of the **source regions 43** (*i.e.*, "*said source region*"). This is just as in the '112 patent, as shown below by the side-by-side comparison with the '112 patent's Figure 3. Thus, *Ueno*'s **source electrode 47** is "*a conformal layer of metal extending laterally across said gates and said source region*." EX1028, ¶105.



EX1003, FIG. 1 (annotated)



EX1001, FIG. 3 (annotated)

Thus, *Ueno* renders obvious claim 3. EX1028, ¶106.

3. Claim 4

a) 4[preamble]: "A silicon carbide MOSFET structure, comprising:"

Ueno discloses element 4[preamble] for the same reasons as element 2[preamble]. EX1028, ¶108.

b) 4[a]: "a silicon carbide wafer having a substrate body having a source region formed adjacent an upper surface thereof;"

Ueno discloses element 4[a] for the same reasons as element 2[a]. EX1028, ¶109.

c) 4[b]: "first and second oxide layers on said upper surface adjacent said source region;"

Ueno discloses element 4[b] for the same reasons as element 2[b]. EX1028, ¶110.

d) 4[c]: "a polysilicon gate above each of said first and second oxide layers;"

Ueno discloses element 4[c] for the same reasons as element 2[c]. EX1028, ¶111.

e) 4[d]: "a gate oxide layer, thicker than said first and second oxide layers beneath said gates, over each of said gates and the sides thereof;"

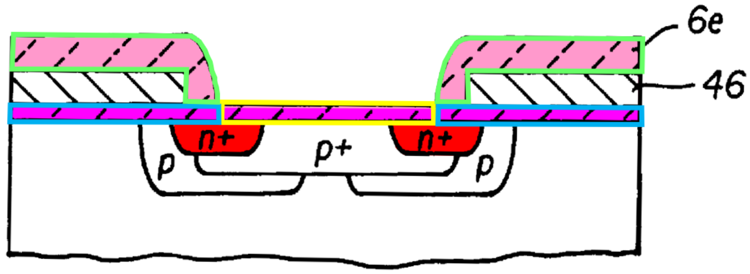
Ueno renders obvious element 4[d] for the same reasons as element 2[d]. EX1028, ¶112.

f) 4[e]: "a metal or oxide layer over said source region, extending between adjacent gate oxide layers; and"

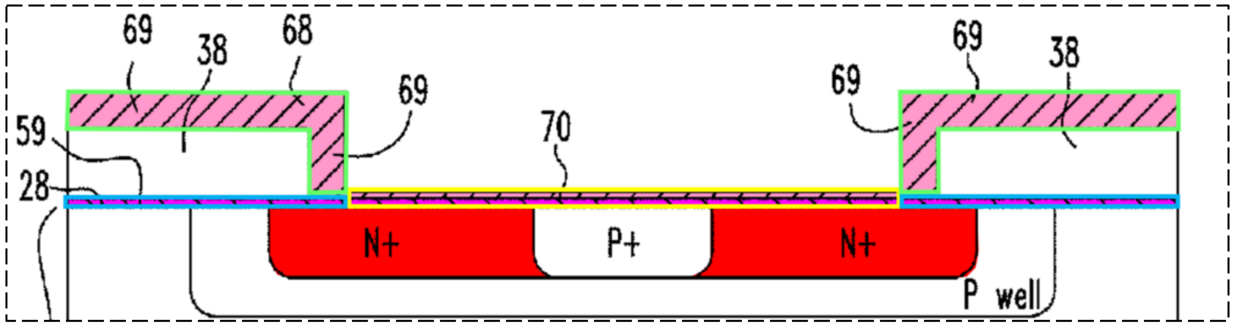
Ueno discloses element 4[e] for the same reasons as element 2[e]. EX1028, ¶113.

g) 4[f]: "wherein said layer over said source region is an oxide layer of greater thickness than said first and second oxide layers and substantially less thickness than said gate oxide layers."

Ueno renders obvious element 4[f]. As discussed above, *Ueno* discloses: for element 2[b], two **gate oxides** corresponding to "*said first and second oxide layers*"; for element 2[d], an **interlayer insulating film 49** over each of the gates corresponding to "*said gate oxide layers*"; and, for element 2[e], "*an oxide layer over said source region, extending between adjacent gate oxide layers*." In Figure 3e below, the **gate oxides** are outlined in light blue, the **interlayer insulating films 49** in light green, and the **oxide layer** over the **source region 43** in yellow. These oxide layers are just like those illustrated in the '112 patent's Figure 7, reproduced and annotated below next to *Ueno*'s Figure 3e for comparison. EX1028, ¶114.



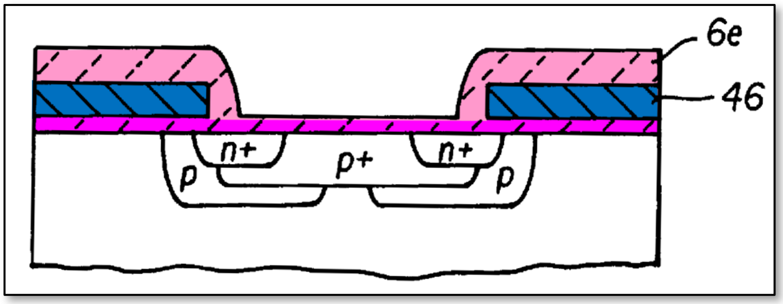
EX1003, FIG. 3e (annotated)



EX1001, FIG. 7 (excerpted and annotated)

As explained in Section X.A.1.e.iii, *Ueno*'s **interlayer insulating film 49** is thicker than its two **gate oxides**. EX1003, 8:29–32. Further, a POSITA would have understood that *Ueno*'s **oxide layer** is of greater thickness than the **gate oxides** and substantially less thickness than the **interlayer insulating films 49**. EX1028, ¶115.

Ueno describes the formation of its **gate oxides**, **interlayer insulating film 49**, and **oxide layer**. As explained in Section X.A.1.e.iii, *Ueno* goes through several fabrication steps. At one stage, a thermal oxidation (at 1100°C. for five hours by a pyrogenic method) forms an **oxide film 6e** over the **gates** and the surface of the SiC substrate between the gates, as *Ueno* illustrates in Figure 3e (below). *Id.*, 10:43–46. EX1028, ¶116.



EX1003, FIG. 3e (annotated)

A POSITA would have understood that, during the above dry oxidation step, the SiC substrate, which is underneath the portion of the **gate oxide film 45** between the **gates**, oxidizes—by reacting with oxygen that diffuses across the already present **gate oxide film 45**—to form silicon dioxide at a much slower rate than the silicon dioxide that grows from the exposed polysilicon **gates**. For instance, Song's article titled "Modified Deal Grove model for the thermal oxidation of silicon carbide," published online on April 16, 2004, four years before the priority date of the '112 patent, explains that the thermal oxidation of SiC includes "in-diffusion of oxygen through the oxide film," "reaction with SiC at the oxide/SiC interface," "[o]ut-diffusion of product gases (e.g., CO) through the oxide film," and "removal of product gases away from the oxide surface." EX1024, 4953. According to Song, "[t]he oxidation of SiC is about one order of magnitude slower than that of Si under the same conditions." *Id.* Song illustrates oxide thickness versus oxidation time for dry oxidation of SiC in Figures 3–5. *Id.*, 4955. On the other hand, Saraswat's 1982 article, titled "Thermal Oxidation of Heavily Phosphorus-Doped Thin Films of

Polycrystalline Silicon," graphs oxide thickness versus oxidation time for dry O_2 oxidation of polysilicon films in Figure 1. EX1025, 2322. A POSITA, comparing Saraswat's Figure 1 to Song's Figures 3–5, would have appreciated that oxide grown from a polysilicon film at 1100°C for five hours would be much thicker than oxide grown from a SiC substrate that is already covered by 30 or 50 nm of oxide layer. *Id.*; EX1024, 4955. As such, a POSITA would have understood that, after *Ueno*'s dry thermal oxidation, there is a slight increase in thickness of the oxide (which includes **gate oxide film 45**) between the **gates** and above the **source regions 43**, resulting in the **oxide layer** being of greater thickness than the two **gate oxides** and substantially less thickness than the **interlayer insulating films 49**. Therefore, *Ueno* renders obvious element 4[f]. EX1028, ¶117.

Accordingly, *Ueno* renders obvious claim 4. EX1028, ¶118.

4. Claim 5

a) 5[preamble]: "A silicon carbide MOSFET structure, comprising:"

Ueno discloses element 5[preamble] for the same reasons as element 2[preamble]. EX1028, ¶120.

b) 5[a]: "a silicon carbide wafer having a substrate body having a source region formed adjacent an upper surface thereof;"

Ueno discloses element 5[a] for the same reasons as element 2[a]. EX1028, ¶121.

c) 5[b]: "first and second oxide layers on said upper surface adjacent said source region;"

Ueno discloses element 5[b] for the same reasons as element 2[b]. EX1028, ¶122.

d) 5[c]: "a polysilicon gate above each of said first and second oxide layers;"

Ueno discloses element 5[c] for the same reasons as element 2[c]. EX1028, ¶123.

e) 5[d]: "a gate oxide layer, thicker than said first and second oxide layers beneath said gates, over each of said gates and the sides thereof;"

Ueno renders obvious element 5[d] for the same reasons as element 2[d]. EX1028, ¶124.

f) 5[e]: "a metal or oxide layer over said source region, extending between adjacent gate oxide layers; and"

Ueno discloses element 5[e] for the same reasons as element 2[e]. EX1028, ¶125.

g) 5[f]: "wherein said MOSFET structure has a first state in which said layer over said source region is an oxide layer of greater thickness than said first and second oxide layers and substantially less thickness than said gate oxide layers, and a second state in which said layer over said source region is a conformal layer of metal extending laterally across said gates and said source region."

i. 5[f1]: "a first state in which said layer over said source region is an oxide layer of greater thickness than said first and second oxide layers and

substantially less thickness than said gate oxide layers"

Ueno renders obvious element 5[f1]. For the same reasons explained above for element 4[f], a POSITA would have appreciated that *Ueno*'s intermediate MOSFET of Figure 3e (*i.e.*, "*a first state*") includes an **oxide layer** over **source regions 43** (*i.e.*, oxide layer "*over said source region*") of greater thickness than the **gate oxides** (*i.e.*, "s*aid first and second oxide layers*") and substantially less thickness than the **interlayer insulating films 49** (*i.e.*, "*said gate oxide layers*"). *See* Section X.A.3.g. *Ueno*'s intermediate structure corresponds to the '112 patent's intermediate structure in the fabrication of MOSFET 21 shown in Figure 7 (*i.e.*, "*a first state*"), in which the oxide layer (combination of a portion of oxidation layer 59 and portion 70 of oxidation layer 68) over **source regions 31 and 32** (*i.e.*, oxide layer "*over said source region*") is of greater thickness than the **oxidation layer 59** underneath the gates 38 (*i.e.*, "s*aid first and second oxide layers*") and substantially less thickness than **portions 69 of the oxidation layer 68** (*i.e.*, "*said gate oxide layers*"). *See* Section VII.A.2. EX1028, ¶126.

ii. 5[f2]: "a second state in which said layer over said source region is a conformal layer of metal extending laterally across said gates and said source region"

Ueno discloses element 5[f2]. As discussed for claim 3, in *Ueno*'s MOSFET structure of Figure 1 (*i.e.*, "*a second state*"), the **source electrode 47** is "*a conformal*

layer of metal extending laterally across said gates and said source region." *See* Section X.A.2. *Ueno's* MOSFET structure corresponds to the '112 patent's MOSFET 21 of Figure 3 (*i.e.*, "*a second state*"), where the **contact metal 45** extends laterally across **gates 38** and **source contacts 31 and 32**. *See* Section VII.A. EX1028, ¶127.

Therefore, *Ueno* render obvious claim 5.[7] *Id.*, ¶128.

5. Claim 6

Independent claim 6 is not challenged in the present petition. The following analysis of claim 6 in view of *Ueno* is provided as basis for the analysis of dependent claims 8, 9, and 13–16, which ***are*** challenged herein. EX1028, ¶129.

a) 6[preamble]: "A MOSFET structure, comprising:"

Regardless of whether the preamble is limiting, *Ueno* discloses it for the same reasons as element 2[preamble]. EX1028, ¶130.

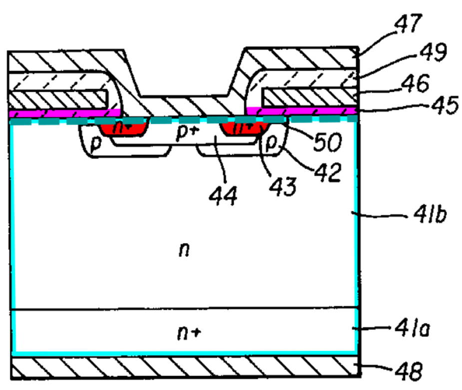
b) 6[a]: "a silicon carbide wafer having a substrate body with an upper surface, said substrate body having at least one source region formed adjacent said upper surface;"

Ueno discloses element 6[a] for the same reasons as element 2[a]. EX1028, ¶131.

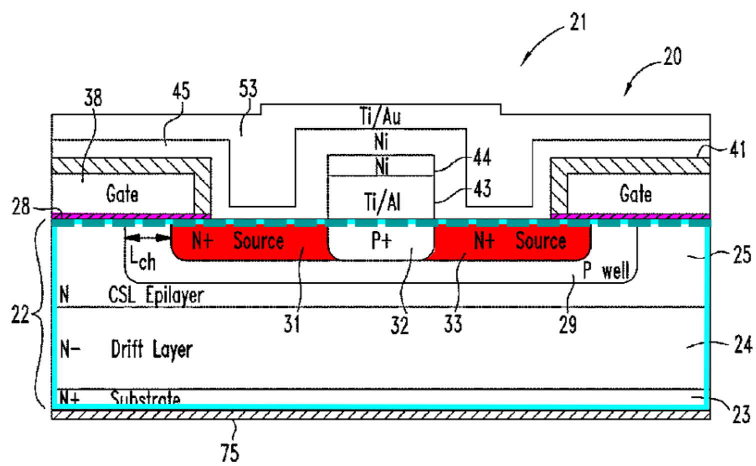
[7] Petitioner reserves the right to challenge claim 5 under 35 U.S.C. § 112 in the related district court litigation should PO assert claim 5.

c) *6[b]: "a substrate surface oxidation layer on said upper surface of said substrate body and adjacent said source region;"*

Ueno discloses element 6[b]. *Ueno* discloses **gate oxides** (magenta below) formed from gate oxide film 45 on the **upper surface** of the **wafer** and adjacent the **source regions 43**. EX1003, 8:7 ("gate oxide film 45"). In both *Ueno* and the '112 patent, there is an **oxidation layer** on the **upper surface** and adjacent the **source regions**, as shown by the side-by-side comparison below of *Ueno*'s Figure 1 with the '112 patent's Figure 3. EX1028, ¶132.



EX1003, FIG. 1 (annotated)



EX1001, FIG. 3 (annotated)

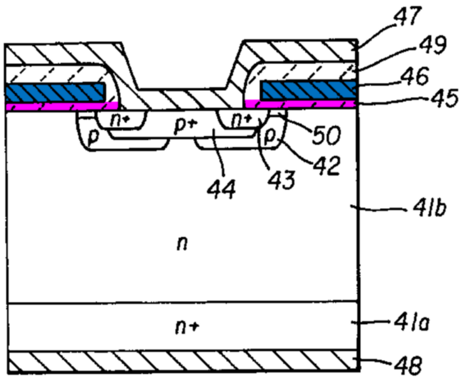
As discussed in Section X.A.1.c, *Ueno*'s two **gate oxides** are formed when a portion of the **gate oxide film 45** above the **source regions 43** is etched away. Either one of these two **gate oxides** corresponds to "*a substrate surface oxidation layer on said upper surface of said substrate body and adjacent said source region.*" EX1028, ¶133.

d) 6[c]: "at least two polysilicon gates above said substrate surface oxidation layer, said gates each having a top, a bottom and sides, wherein a first source region of said at least one source region is juxtaposed between first and second adjacent gates of said at least two polysilicon gates;"

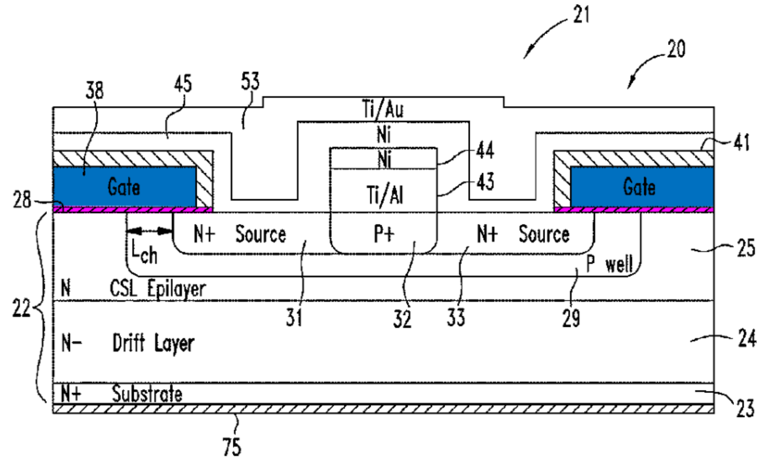
Ueno renders obvious element 6[c]. As explained below, *Ueno* explicitly discloses two **gates** that are above the **gate oxide film 45** (*i.e.*, "*said substrate surface oxidation layer*"). EX1003, 8:6–7 ("gate electrode layer 46 made of polysilicon is formed on a gate oxide film 45"). Moreover, each of the two **gates** has a **top**, a **bottom**, and a **side**, as also explained below. As illustrated in *Ueno*'s Figure 1 below, either one of the **source regions 43** is also juxtaposed between the two **gates**. EX1028, ¶134.

i. 6[c1]: "at least two polysilicon gates above said substrate surface oxidation layer"

Ueno discloses element 6[c1]. *Ueno* discloses two polysilicon **gates** (blue). Further, *Ueno*'s Figure 1 (alongside the '112 patent's Figure 3 for comparison) shows the **gates** above the **gate oxide film 45** (*i.e.*, "*said substrate surface oxidation layer*"). EX1028, ¶135.

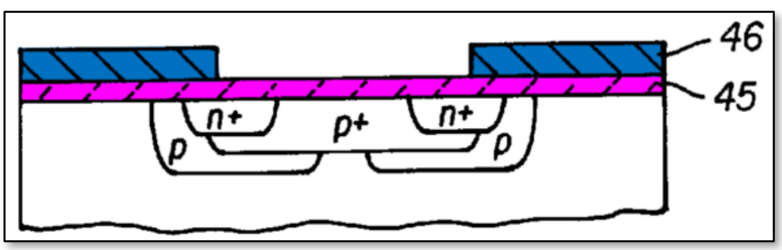


EX1003, FIG. 1 (annotated)



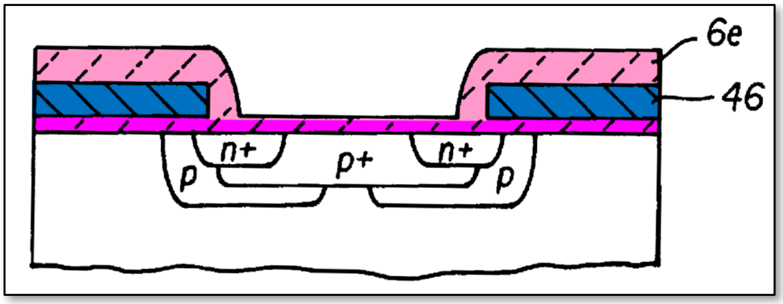
EX1001, FIG. 3 (annotated)

As *Ueno* explains when describing the process steps for manufacturing the MOSFET of Figure 1, a polysilicon film 1c is deposited on the **gate oxide film 45** and patterned to provide the gate electrode layer 46, forming the **gates**. EX1003, 7:37–39, 10:39–44, Figures 3c and 3d. *Ueno*'s Figure 3d (below) shows the two **gates** above the **gate oxide film 45**. EX1028, ¶136.



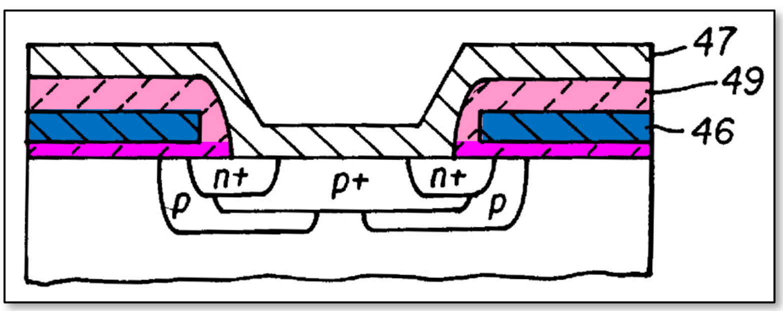
EX1003, FIG. 3d (annotated)

Thereafter, thermal oxidation forms an **oxide film 6e** over the **gates** and the surface of the SiC substrate, as *Ueno* illustrates in Figure 3e (below). *Id.*, 10:43–46. EX1028, ¶137.



EX1003, FIG. 3e (annotated)

Subsequently, the oxide film 6e is subjected to etching to expose an electrode contact portion. *Id.*, 10:48–51. During the same etching process, as can be seen in *Ueno*'s Figure 3f (below), a portion of the **gate oxide film 45** between the **gates** gets etched away, leaving behind the two **gate oxides**. As a result, the two **gates** remain above the **gate oxides**. EX1028, ¶138.

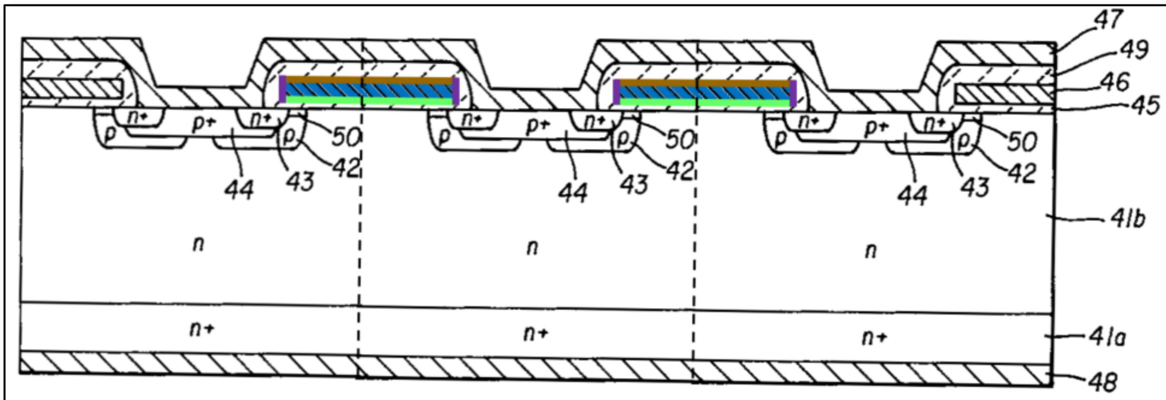


EX1003, FIG. 3f (annotated)

ii. *6[c2]: "said gates each having a top, a bottom and sides"*

Ueno renders obvious element 6[c2]. As discussed in Section X.A.e.i, per *Ueno*'s teaching of "unit cell" and "pitch of the unit cells" as would be understood by a POSITA and as illustrated and taught by *Grant*, multiple copies of *Ueno*'s unit

cell of Figure 1 may be depicted side by side as shown below. *Ueno* explicitly discloses that each of its two **gates** in Figure 1 has a **top** (outlined in brown) and a **bottom** (outlined in lime). As also discussed in Section X.A.e.i, a POSITA would have recognized that each gate would have had two **sides** (outlined in purple). EX1028, ¶139.

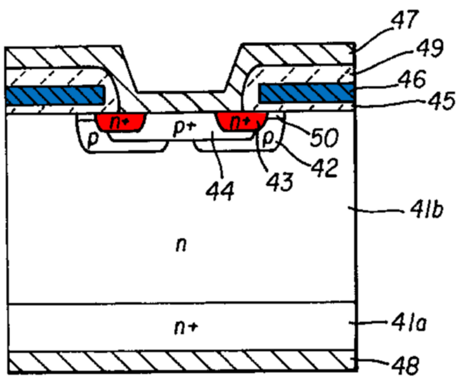


EX1003, FIG. 1 (replicated and annotated)

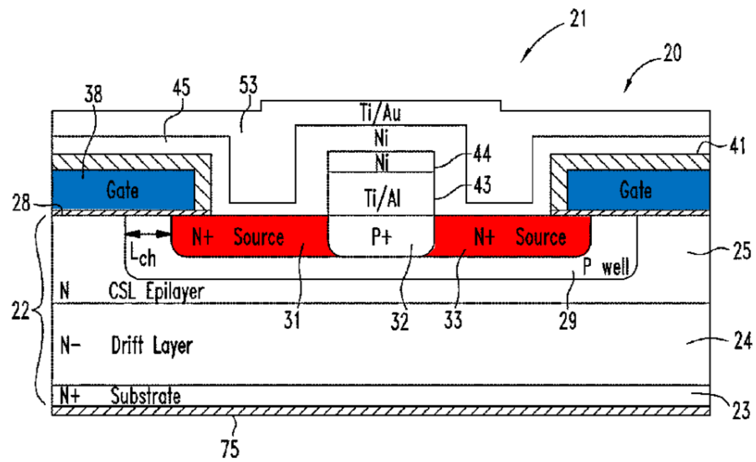
iii. ***6[c3]: "a first source region of said at least one source region is juxtaposed between first and second adjacent gates of said at least two polysilicon gates"***

Ueno discloses element 6[c3]. As illustrated in *Ueno*'s Figure 1 below, either one of the **source regions 43** is positioned between (i.e., "*juxtaposed*") the two **gates** 46. EX1003, 8:6–10 ("A ***gate electrode layer 46 made of polysilicon*** is formed on a gate oxide film 45, over the surface of the p base region 42 that is interposed between the ***n^+ source region 43*** and the exposed surface portion of the n drift layer

41b."), 10:21–24, 10:42–44. Because there is no intervening gate between the two **gates**, they are adjacent each other. A side-by-side comparison below with the '112 patent's Figure 3 shows that, in both *Ueno* and the '112 patent, the **source regions** are between the two **gates**. Thus, *Ueno* discloses element 6[c3]. EX1028, ¶140.



EX1003, FIG. 1 (annotated)



EX1001, FIG. 3 (annotated)

e) 6[d]: "a gate oxide layer, thicker than said substrate surface oxidation layer, over said tops and sides of each of said gates; and"

Ueno discloses element 6[d] for the same reasons as element 2[d]. EX1028, ¶141.

f) 6[e]: "a material layer over said first source region and between said gate oxide layers on said sides of said gates, said material layer comprising one of an oxide and a metal contact."

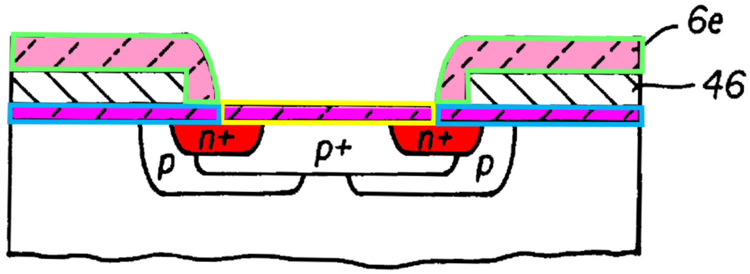
Ueno discloses element 6[e] for the same reasons as element 2[e]. EX1028, ¶142.

Therefore, *Ueno* renders obvious claim 6. *Id.*, ¶143.

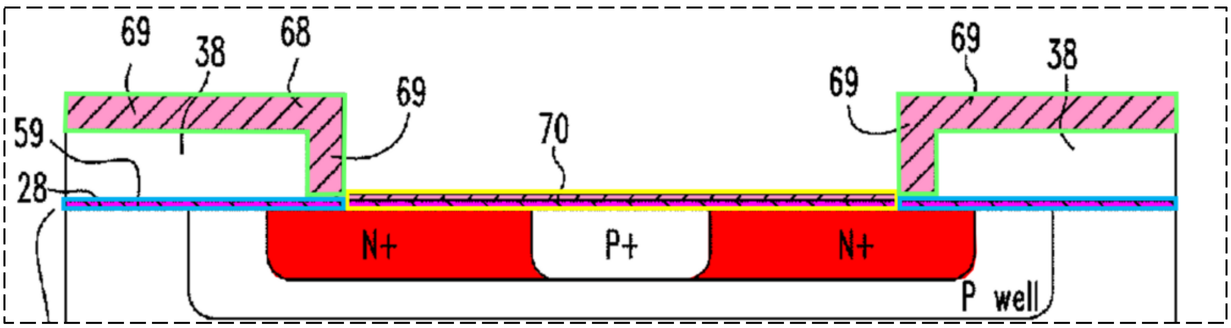
6. Claim 8

> ***"The MOSFET structure of claim 6, wherein said material layer is a source oxide layer having a thickness greater than that of said substrate surface oxidation layer and less than that of said gate oxide layer."***

Ueno renders obvious claim 6, as discussed above. *Ueno* also renders obvious the additional limitation of claim 8. As discussed for element 6[b], *Ueno* discloses two **gate oxides**, either of which corresponds to "*said substrate surface oxidation layer*" and, for element 2[d], an **interlayer insulating film 49** over each of the gates corresponding to "*said gate oxide layer*." Moreover, for the same reasons explained above for element 4[f] above, a POSITA would have appreciated that *Ueno*'s intermediate MOSFET of Figure 3e (below) includes an **oxide layer** (outlined in yellow) of greater thickness than the **gate oxides** (outlined in light blue) and substantially less thickness than the **interlayer insulating films 49** (outlined in light green). *See* Section X.A.3.g. *Ueno*'s **oxide layer** is "*a source oxide layer*." The '112 patent's Figure 7 is reproduced and annotated below next to *Ueno*'s Figure 3e for comparison. As can be seen, *Ueno*'s **oxide layer** is over its **source regions** (red), just like the '112 patent's oxide layer, which is outlined in yellow below (*i.e.*, combination of a portion of oxidation layer 59 and portion 70 of oxidation layer 68), is over its **source contacts**. EX1028, ¶144.



EX1003, FIG. 3e (annotated)



EX1001, FIG. 7 (excerpted and annotated)

Therefore, *Ueno* renders obvious claim 8. EX1028, ¶145.

7. Claim 9

> ***"The MOSFET structure of claim 8, wherein said source oxide layer includes a first layer homogeneously formed with and of the same thickness as said substrate surface oxidation layer and a second, separately formed layer homogeneously formed with and of lesser thickness than said gate oxide layer."***

Ueno renders obvious claim 8, as discussed above. *Ueno* also renders obvious the additional limitation of claim 9. As discussed for claim 8, *Ueno*'s **oxide layer** corresponds to "*said source oxide layer*." For the same reasons described above for element 4[f] above, a POSITA would have appreciated that *Ueno*'s **oxide layer** is the combination of a portion of **gate oxide film 45** and the additional oxide that

grows when the SiC substrate underneath the **gate oxide film 45** oxidizes. *See* Section X.A.3.g. The **gate oxide film 45** is "*a first layer*" that is homogeneously formed with and of the same thickness as the gate oxides (*i.e.*, "*said substrate surface oxidation layer*") because the gates oxides are formed from the same **gate oxide film 45**, as explained above for limitation 6[b]. The additional oxide layer grown from oxidization of the SiC substrate is "*a second layer*" formed separately from the **gate oxide film 45**. Moreover, as explained above for element 4[f], the additional oxide layer is formed homogeneously with and of less thickness than the than the **interlayer insulating films 49** ("*said gate oxide layer*") because both are formed during the same oxidization step and the oxidization rate is faster for polysilicon than for SiC. *See* Section X.A.3.g. EX1028, ¶146.

Therefore, *Ueno* renders obvious claim 9.[8] *Id.*, ¶147.

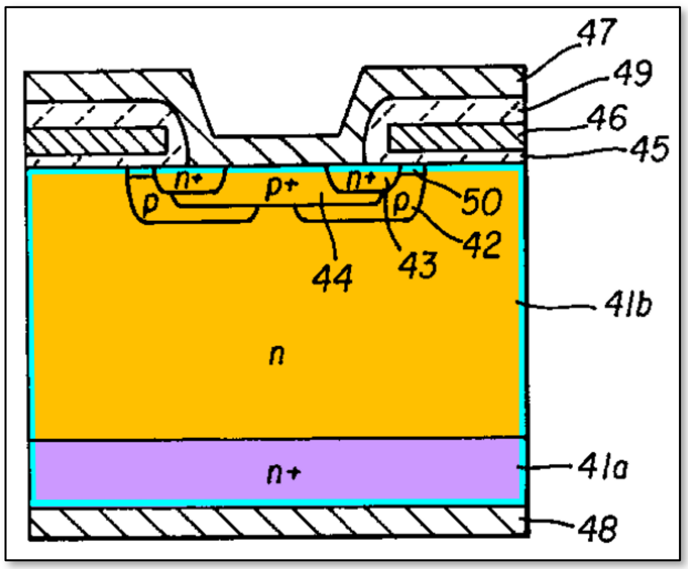
8. Claim 13

> ***"The MOSFET structure of claim 6, wherein said substrate body includes a lower, heavily doped substrate and a lightly doped superjacent drift layer."***

Ueno renders obvious claim 6, as discussed above. *Ueno* also discloses the additional limitation of claim 13. For example, *Ueno* discloses that "the n **drift layer**

[8] Petitioner reserves the right to challenge claim 9 under 35 U.S.C. § 112 in the related district court litigation should PO assert claim 9.

41b doped with phosphorous is epitaxially ***grown on*** the n+ drain **layer 41a**, to provide a 4H-SiC substrate." *Id.*, 8:54–56. *Ueno* uses "drain layer" and "substrate" interchangeably to refer to layer 41a. *Id.*, 8:12–13 ("n+ drain layer or substrate 41a"). As can be seen in *Ueno*'s annotated Figure 1 below, the **drift layer 41b** is superjacent (*i.e.*, overlying) the lower **substrate layer 41a** and they are both included in the **wafer** (*i.e.*, "*said substrate body*"). EX1028, ¶148.



EX1003, FIG. 1 (annotated)

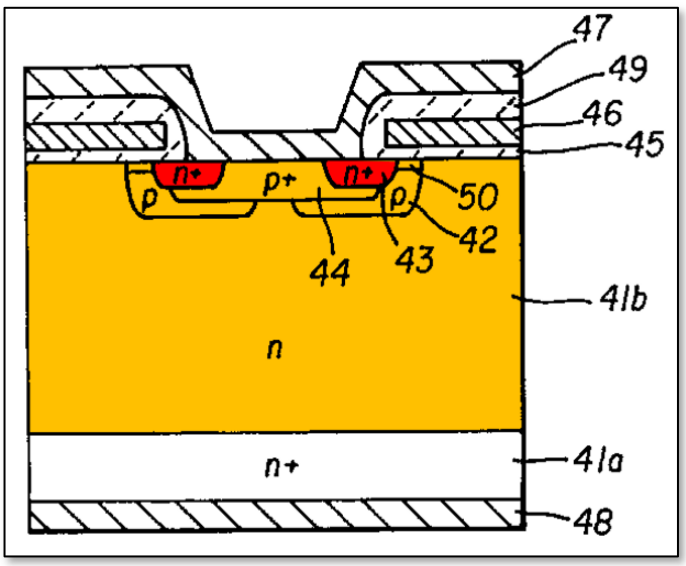
Moreover, *Ueno* also discloses that "the n+ drain **layer 41a** has an impurity concentration of 1×10^{18} cm^{-3} . . . and the n **drift layer 41b** has an impurity concentration of 1×10^{16} cm^{-3}." *Id.*, 8:18–20. Thus, the **substrate 41a** is heavily doped and the **drift layer 41b** is lightly doped. EX1028, ¶149.

Thus, *Ueno* renders obvious claim 13. *Id.*, ¶150.

9. Claim 14

"The MOSFET structure of claim 13, wherein said at least one source region is defined in said drift layer."

Ueno renders obvious claim 13, as discussed above. *Ueno* also discloses the additional limitation of claim 14. For example, *Ueno*'s **source regions 43** (*i.e.*, "*said at least one source region*") are defined in its **drift layer 41b** (*i.e.*, "*said drift layer*"). *See also* EX1003, 9:59–62, 10:21–24, Figures 2g and 3b; Section X.A.1.b.iii (explaining how nitrogen atoms are implanted into the **drift layer 41b** and activated to form the **source regions 43**). EX1028, ¶151.



EX1003, FIG. 1 (annotated)

Thus, *Ueno* renders obvious claim 14. EX1028, ¶152.

B. Ground II: Claims 15 and 16 are Obvious over *Ueno* in View of *Cooper*

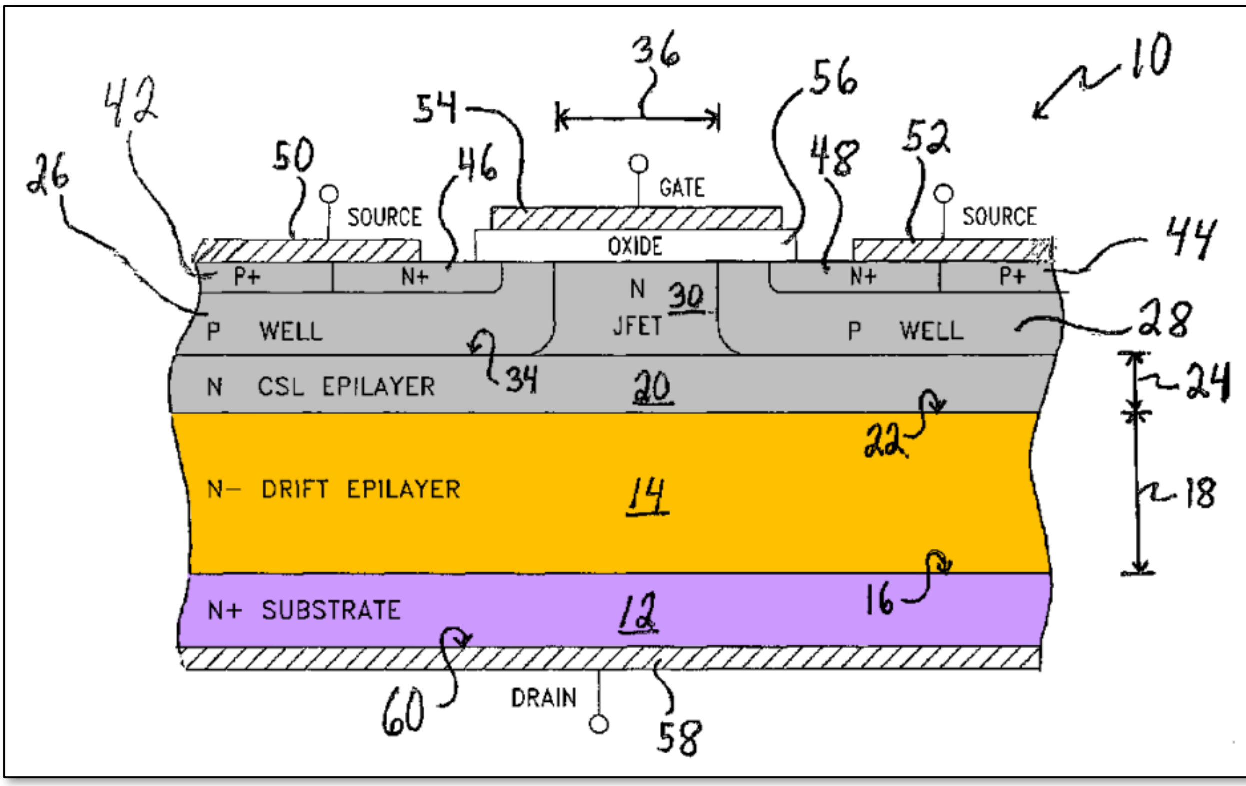
1. Claim 15

> ***"The MOSFET structure of claim 6, wherein said substrate body includes a lower, heavily doped substrate, a lightly doped drift layer superjacent to said substrate, and a current spreading layer (CSL) that is superjacent to said drift layer and that is more heavily doped than said drift layer, but not as heavily doped as said substrate."***

Ueno renders obvious claim 6, as discussed in Ground I. The combination of *Ueno* and *Cooper* renders obvious the additional limitation of claim 15. EX1028, ¶153.

As discussed in Ground I for claim 13, *Ueno* discloses "*said substrate body includes a lower, heavily doped substrate and a lightly doped superjacent drift layer*." *Ueno* does not explicitly disclose "*a current spreading layer (CSL) that is superjacent to said drift layer and that is more heavily doped than said drift layer, but not as heavily doped as said substrate*," but *Cooper* does. Specifically, *Cooper* discloses and illustrates in Figure 1 (below) a semiconductor device 10 that includes a **current spreading layer (CSL) 20** (grey) overlying a **drift layer 14** (orange), which overlies a **substrate 12** (lavender). EX1026, ¶17 ("semiconductor device 10 includes a substrate 12"), ¶18 ("semiconductor device 10 includes a drift semiconductor layer 14 formed on a front side 16 of the substrate 12"), ¶21 ("semiconductor device 10 also includes a current spreading semiconductor layer 20

formed on a front side 22 of the drift layer 14"); *see also id*, ¶24 ("growing an extra-thick current spreading layer 20 and forming the 'P' wells 26, 28 using a suitable incorporation process such as an ion implantation process."). EX1028, ¶154.



EX1026, FIG. 1 (annotated)

Cooper discloses that the **substrate 12** is "doped with an N-type impurity to an '**N+**' concentration," the **drift layer 14** is "doped with N-type impurities to an '**N−**' concentration," and the **CSL 20** is "doped with N-type impurities to an "**N**" concentration." *Id.*, ¶¶ 17, 19, 21. *Cooper* further discloses that "the **current spreading layer 20** may be doped to an N-type impurity concentration that is one order of magnitude or greater than the doping concentration of the **drift layer 14**."

Id., ¶21. In particular, *Cooper* discloses that "the **drift layer 14** has a doping concentration of about 1×10^{16} cm^{-3} and the **current spreading layer 20** has a doping concentration of about 1×10^{17} cm^{-3}." *Id.* Although *Cooper* does not disclose a specific doping concentration for the **substrate 12**, a POSITA would have understood an "N" concentration to be lower than an "N+" concentration. *See, e.g.*, EX1009, 26–27 (designating regions that are heavily doped with donors as n+ to indicate where impurity concentration exceeds about 10^{18} cm^{-3}). Therefore, *Cooper* discloses "*a current spreading layer (CSL) that is superjacent to said drift layer and that is more heavily doped than said drift layer, but not as heavily doped as said substrate*." EX1028, ¶155.

i. Motivation to Combine Ueno and Cooper

A POSITA would have been motivated to modify *Ueno*'s **wafer** according to and informed by *Cooper*'s teachings to include a current spreading layer (CSL) that overlies the **drift layer 41b** and that is more heavily doped than the **drift layer 41b**, but not as heavily doped as the **substrate layer 41a**. In particular, as explained below, a POSITA would have been motivated to include *Cooper*'s CSL in *Ueno* to obtain a lower on-resistance. Further, that combination would have been achievable by a POSITA with no unexpected results. EX1028, ¶156.

Ueno and *Cooper* are from the same field of endeavor as the '112 patent's claims. *See, e.g.*, *Medtronic, Inc. v. Cardiac Pacemakers, Inc.*, 721 F.2d 1563,

1574–75 (Fed. Cir. 1983); M.P.E.P. § 2141. Both references are directed to SiC vertical power MOSFETs. *Ueno* discloses "a method for manufacturing silicon carbide vertical MOS semiconductor devices having high breakdown voltage." EX1003, 4:45–46. Similarly, *Cooper* discloses "semiconductor devices for high-voltage power applications," in particular a "vertical double-implanted metal-oxide semiconductor field-effect transistor." EX1026, ¶¶2, 9, 17. Moreover, *Cooper* claims the benefit of "U.S. Provisional Patent Application Ser. No. 60/646,152 entitled 'Optimized Vertical Power DMOSFETs in Silicon Carbide.'" *Id*., ¶1. Thus, both references are directed to SiC vertical power MOSFETs and aim at improving their characteristics. EX1028, ¶157.

Implementing *Ueno*'s **wafer** to include a CSL that overlies the **drift layer 41b** and that is more heavily doped than the **drift layer 41b**, but not as heavily doped as the **substrate layer 41a** as taught by *Cooper* would have yielded expected, predictable results. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007); M.P.E.P. 2143(I)(A). *Ueno* discloses its **drift layer 41b** overlying its **substrate layer 41a**. EX1003, 8:54–56. *Ueno* also discloses that the **substrate 41a** has a doping concentration of 1×10^{18} cm^{-3} that is higher than the doping concentration of 1×10^{16} cm^{-3} of the **drift layer 41b**. *Id.*, 8:18–20. Similarly, *Cooper* discloses that its **drift layer 14** with an "N−' concentration overlies its **substrate 12** with an "N+" concentration. EX1026, ¶¶17–19. Moreover, *Cooper* discloses a **CSL 20** with an

"N" concentration layer overlying its **drift layer 14**. *Id.*, ¶21. In particular, *Cooper* discloses that "the **drift layer 14** has a doping concentration of about 1×10^{16} cm^{-3} and the **current spreading layer 20** has a doping concentration of about 1×10^{17} cm^{-3}." *Id.* A POSITA would have combined the elements taught by *Ueno* and *Cooper*—namely, the **drift layer 41b** overlying the **substrate layer 41a** as taught by *Ueno*, and the **CSL 20** overlying the **drift layer 14**, which overlies the **substrate 12** as taught by *Cooper*—using known and routine semiconductor fabrication techniques to modify *Ueno*'s **wafer** to include a CSL that overlies the **drift layer 41b** and that is more heavily doped than the **drift layer 41b**, but not as heavily doped as the **substrate layer 41a**. This result would have been readily predictable and recognized by a POSITA because, as *Cooper* teaches, "by forming the **current spreading layer 20**, the specific on-resistance of the semiconductor device 10 may also be reduced ***compared to a MOSFET device without a current spreading layer.***" *Id.*, ¶27. *Cooper* explains that "[b]ecause the doping concentration of the **current spreading layer 20** is greater than the doping concentration of the underlying **drift layer 14**, current tends to flow downwardly from the JFET region 30 and laterally through the **current spreading layer 20** before subsequently flowing down through the upper portion of the lower doped **drift layer 14**" and "[b]ecause the current tends to flow laterally through the **current spreading layer 20**, the current density of the semiconductor device 10 through the

lower doped **drift layer 14** may be reduced thereby reducing the specific on-resistance of the semiconductor device 10." *Id.* A POSITA, knowing the importance of reducing on-resistance to minimize voltage drop when a MOSFET is ON, would have appreciated, from *Cooper*'s teachings, that the addition of a CSL would reduce the on-resistance of a MOSFET. *See, e.g.*, EX1009, 18 ("minimization of the ON-state voltage drop is an important consideration in power devices"). Thus, a POSITA would have been motivated to modify *Ueno*'s **wafer** to include a CSL that overlies the **drift layer 41b**. EX1028, ¶158.

A POSITA would have been further motivated to combine the teachings of *Ueno* and *Cooper* because it would have simply provided the simple substitution of one known element (the **drift layer 41b** overlying the **substrate layer 41a** in *Ueno*) for another (the **CSL 20** overlying the **drift layer 14**, which overlies the **substrate 12** as taught by *Cooper*) to obtain predictable results. *KSR*, 550 U.S., 416; M.P.E.P. 2143(I)(B). This substitution would have been readily achievable by a POSITA via known and routine semiconductor fabrication techniques to implement *Ueno*'s **wafer** to include a CSL that overlies the **drift layer 41b** and that is more heavily doped than the **drift layer 41b**, but not as heavily doped as the **substrate layer 41a**. EX1028, ¶159.

The modification of *Ueno*'s **wafer** to include a CSL that overlies the **drift layer 41b** and that is more heavily doped than the **drift layer 41b**, but not as heavily

doped as the **substrate layer 41a** as taught by *Cooper* would have been readily implemented by modifying *Ueno*'s fabrication process to include an additional epitaxial layer. A POSITA could have achieved this modification using basic semiconductor fabrication techniques to grow an additional epitaxial layer over *Ueno*'s **drift layer 41b** and doping this additional layer such that it is more heavily doped than the **drift layer 41b**, but not as heavily doped as the **substrate layer 41a**, thereby forming a CSL. This modification would have been well within the knowledge and skillset of a POSITA. EX1028, ¶160.

ii. Reasonable Expectation of Success in Combining Ueno and Cooper

A POSITA would also have had a reasonable expectation of success. The combination of *Ueno* and *Cooper* represents a straight-forward implementation of steps of the well-understood semiconductor fabrication processes to grow semiconductor layers with different doping concentrations, which a POSITA would have been familiar with and been able to implement. The reasons a POSITA would have expected success parallel those that provide motivation for this combination—including because both *Ueno* and *Cooper* are directed to SiC vertical power MOSFETs. EX1003, 4:45–46, Figure 1; EX1026, ¶¶1, 2, 9, 17, Figure 1. A POSITA would have had a reasonable expectation of success in modifying *Ueno*'s **wafer** to include a CSL per the teachings of *Cooper* because both *Ueno* and *Cooper*

aim at reducing power loss in high-voltage SiC vertical MOSFETs. EX1003, 12:20–22 ("SiC semiconductor devices having a high breakdown voltage and a reduced loss can be easily produced according to the present invention"); EX1026, ¶27 ("the specific on-resistance of the semiconductor device 10 may also be reduced compared to a MOSFET device"). EX1028, ¶161.

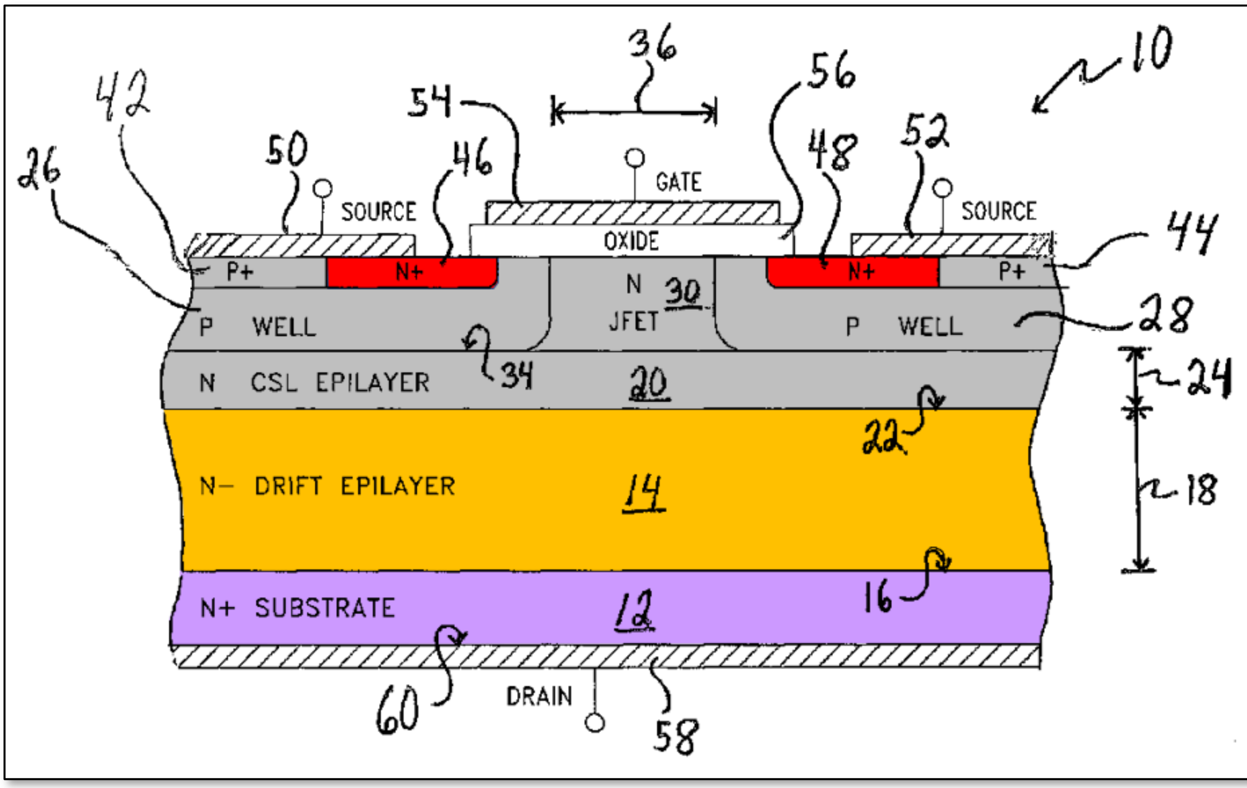
Accordingly, *Ueno* in view of *Cooper* renders obvious claim 15 and a POSITA would have been motivated to combine the teachings of these references and would have had a reasonable expectation of success. EX1028, ¶162.

2. Claim 16

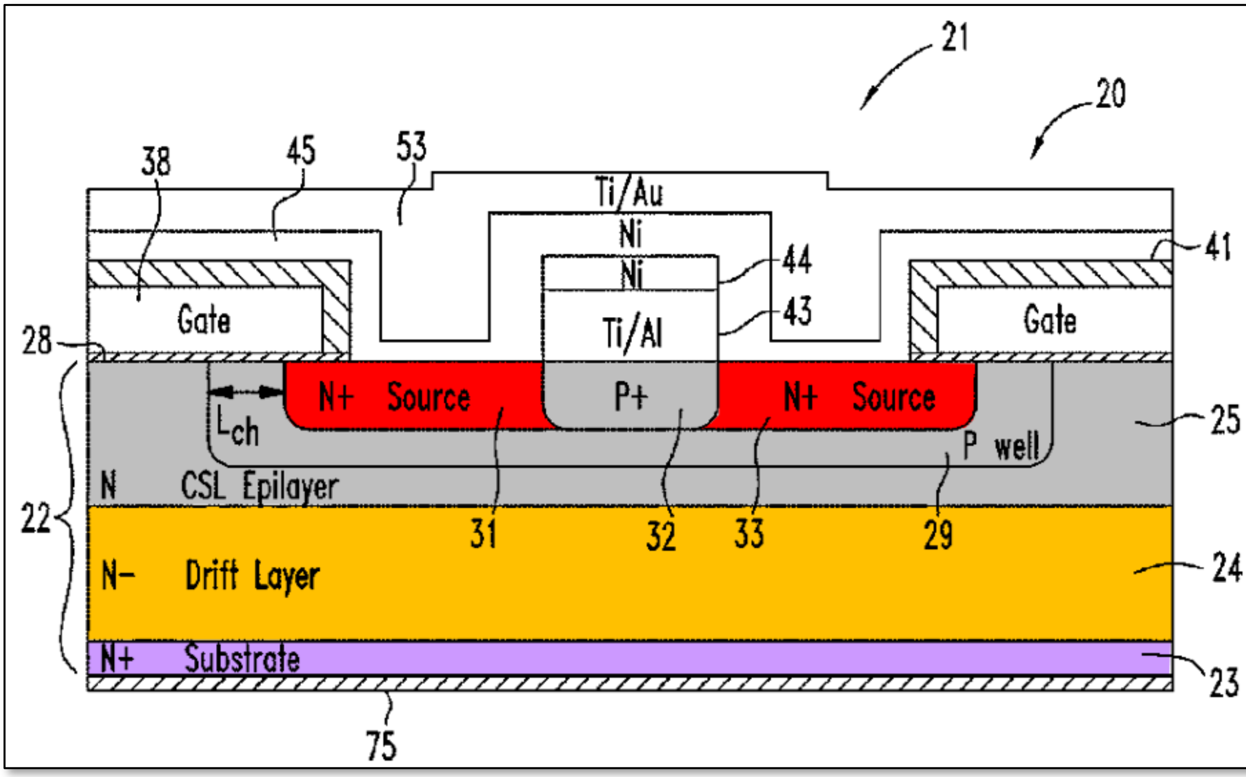
> ***"The MOSFET structure of claim 15, wherein said at least one source region is defined in said current spreading layer (CSL)."***

The combination of *Ueno* and *Cooper* renders obvious claim 15, as discussed above. The combination of *Ueno* and *Cooper* further renders obvious the additional limitation of claim 16. *Cooper* teaches "growing an extra-thick **current spreading layer 20** and forming the 'P' wells 26, 28 using a suitable incorporation process such as an ion implantation process." EX1026, ¶24. As shown in *Cooper*'s annotated Figure 1 below, the **source regions 46, 48** (red) are "defined in the P wells 26 and 28, respectively," which themselves are formed in the **CSL 20**. *Id.*, ¶29. This is just like how the '112 patent forms its **source regions 31 and 32** in its P well 29, which is formed in the **CSL 25**. EX1001, 4:30–31 ("Formed in the top of the current

spreading layer 25 is a P well 29."); 4:51–52 ("Formed within P well 29 are two heavily doped N+ implant source regions 31 and 32"). The '112 patent's Figure 3 is compared with *Cooper*'s Figure 1 below. EX1028, ¶163.



EX1026, FIG. 1 (annotated)



EX1001, FIG. 3 (annotated)

Accordingly, modifying *Ueno*'s **wafer** to include a CSL as taught by *Cooper*—as discussed for claim 15—would result in *Ueno*'s **source regions 43** (formed within p base regions 42) being defined in the CSL. EX1028, ¶164.

Thus, *Ueno* renders obvious claim 16. *Id.*, ¶165.

XI. CO-PENDING DISTRICT COURT LITIGATION IN TEXAS SHOULD NOT PRECLUDE INSTITUTION

Although there is concurrent district court litigation involving the '112 patent, the weight of the factors described in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 5–6 (PTAB Mar. 20, 2020) (precedential) favors institution of this Petition.

A. The potential for a stay of the district court case urges against denial (factor 1)

After at least any institution of review based on this Petition, ST intends to seek a stay of the co-pending district court proceedings. Therefore, factor 1 is neutral because any decision by the district court to stay the case would issue after institution and be based on "a variety of circumstances and facts beyond [the Board's] control and to which the Board is not privy." *See Sand Revolution II, LLC v. Cont'l Intermodal Grp. Trucking, LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative).

B. Uncertainty over the trial date in the Texas case favors institution (factor 2)

The district court recently entered a Scheduling Order identifying April 24, 2023 as the target trial date. EX1015, 5. Based on the expected 18-month IPR schedule, a final written decision (FWD) in this proceeding would likely issue by September 2023. However, this factor favors institution, or is neutral, because the district court's trial date is subject to considerable uncertainty. *Sand Revolution*, IPR2019-01393, Paper 24 at 9-10 (uncertainty of trial date weighed in favor of institution) (informative); *Micron Tech., Inc. v. Godo Kaisha IP Bridge 1*, IPR2020-01008, Paper 10 at 14 (PTAB Dec. 7, 2020).

Despite the district court's aspirational target date, trial is unlikely to begin on April 24, 2023 and may be postponed until after the Board issues a FWD in this

proceeding. *E.g.,* EX1027 (the court's crowded docket, including over 834 pending patent cases); EX1017, 3 ("In the WDTX, 70% of trial dates initially relied upon by the PTAB to deny petitions have slid.").

In contrast to the potential delays to the district court's schedule, the Board's schedule is unlikely to shift. 35 U.S.C. § 316(a)(11) (one-year statutory deadline for FWD); *Sand Revolution*, IPR2019-01393, Paper 24 at 9. Given the circumstances, the Board may well issue a FWD before the beginning of any trial in the district court.

Factor 2 also favors institution because ST diligently filed this Petition ***nearly four months*** before its statutory deadline for doing so. *See, e.g.*, *Apple Inc. v.Seven Networks, LLC*, IPR2020-00156, Paper 10 at 9 & n.8 (PTAB June 15, 2020) (considering the filing date relative to potential filing dates helps to analyze factor 2 on a sliding scale based on relative trial dates).

C. Investment in the parallel district court proceeding is minimal and ST was diligent in filing this Petition (factor 3)

The co-pending district court case is still in an early phase. The court has not addressed the merits of the case. All significant stages of litigation—including discovery, claim construction, summary judgment, and trial—remain in the future. The target trial date is 13 months away and will likely be delayed. After receiving

at least any institution decision, ST intends to move for a stay in the district court to further minimize investment by the court and the parties.

D. The Petition raises unique issues, which favors institution (factor 4)

ST expects its invalidity positions in the district court case will diverge from the ground of unpatentability described in this Petition. At the time of filing this Petition, the claims challenged herein have not been asserted against ST and are not being litigated in the district court. In any event, ST reserves the right to enter a stipulation relating to the district court case that would prevent and/or reduce overlap with the requested IPR, should the Board deem one necessary. *See Sand Revolution*, IPR2019-01393, Paper 24 at 12.

E. The parties overlap (factor 5)

The district court case and the IPR proceeding involve the same parties.

F. The merits of ST's challenge support institution (factor 6)

As described above, *Ueno* renders obvious the allegedly inventive features of the '112 patent, including the configuration recited by claims 2–5, 8, 9, 13, and 14, and the combination of *Ueno* and *Cooper* renders obvious claims 15 and 16. The merits of the prior art and their close correspondence to the challenged claims favors institution. *Fintiv*, IPR2020-00019, Paper 11 at 14–15.

XII. CONCLUSION

Petitioner requests institution of an *inter partes* review of the '112 patent and cancellation of claims 2–5, 8, 9, and 13–16.

Respectfully Submitted,

Dated: March 25, 2022

/Scott Bertulli/
Scott Bertulli, Lead Counsel
Registration No. 75,886

TABLE OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 8,035,112
1002	[Reserved]
1003	U.S. Patent No. 6,238,980 ("*Ueno*")
1004	U.S. Patent No. 5,233,215 ("*Baliga*")
1005	'112 Patent File History, 11/12/2010 Preliminary Amendment
1006	'112 Patent File History, 2/23/2011 Non-Final Office Action
1007	'112 Patent File History, 5/23/2011 Response to Office Action
1008	'112 Patent File History, 6/29/2011 Notice of Allowance
1009	D. A. Grant and J. Gowar, "Power MOSFETs – Theory and Applications," 1989 ("*Grant*") (relevant sections)
1010	U.S. Patent No. 5,510,281 ("*Ghezzo*")
1011	J. A. Cooper, Jr. et al., "Status and Prospects for SiC Power MOSFETs," IEEE Transactions on Electron Devices, vol. 49, no. 4, April 2002
1012	J. A. Cooper, Jr. et al., "SiC Power-Switching Devices—The Second Electronics Revolution?," Proceedings of the IEEE, vol. 90, no. 6, June 2002
1013	U.S. Patent No. 5,317,184 ("*Rexer*")
1014	[Reserved]

Exhibit	Description
1015	Scheduling Order, *The Trustees of Purdue University v. STMicroelectronics, Inc. et al.*, No. 6:21-cv-00727 (W.D. Tex.), Dkt. 45 (November 22, 2021)
1016	[Reserved]
1017	Article entitled "District Court Trial Dates Tend to Slip After PTAB Discretionary Denials" (July 24, 2020)
1018	Y. Xiao et al., "Current Sensing Trench Power MOSFET for Automotive Applications," Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, 2005
1019	U.S. Patent Publication No. 2004/0222483
1020	[Reserved]
1021	P. G. Neudeck, "Progress in Silicon Carbide Semiconductor Electronics Technology," Journal of Electronic Materials, vol. 24, no. 4, 1995
1022	[Reserved]
1023	M. Quirk, et al. "Semiconductor Manufacturing Technology," 2001 (relevant sections)
1024	Y. Song et al., "Modified Deal Grove model for the thermal oxidation of silicon carbide," Journal of Applied Physics, vol. 95, no. 9, 2004
1025	K. Saraswat et al., "Thermal Oxidation of Heavily Phosphorus-Doped Thin Films of Polycrystalline Silicon," Journal of Electrochemical Society, vol. 129, no. 10, 1982
1026	U.S. Patent Application Publication No. 2006/0192256 ("*Cooper*")

Exhibit	Description
1027	Statistics from Docket Navigator showing active patent cases before Judge Alan Albright of the U.S. District Court for the Western Digital of Texas (as of March 25, 2022)
1028	Declaration of Dr. Vivek Subramanian

CERTIFICATE UNDER 37 CFR § 42.24(d)

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,900, which is less than the 14,000 words allowed under 37 CFR § 42.24(a)(1)(i).

Respectfully submitted,

DATED: March 25, 2022

/Scott Bertulli/
Scott Bertulli
Reg. No. 75,886

CERTIFICATE OF SERVICE

I hereby certify that on March 25, 2021, I caused a true and correct copy of the foregoing materials:

- Petition for *Inter Partes* Review of U.S. Patent No. 8,035,112 under 35 U.S.C. § 312 and 37 C.F.R. § 42.104
- Exhibit List
- Exhibits for Petition for *Inter Partes* Review of U.S. Patent No. 8,035,112 (EX1001–EX1028)
- Power of Attorney
- Fee Authorization
- Word Count Certification Under 37 CFR § 42.24(d)

to be served via Express Mail on the following correspondent of record as listed on PAIR:

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DATED: March 25, 2022

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